HIGH FREQUENCY AND HIGH DYNAMIC RANGE

CONTINUOUS TIME FILTERS

A Dissertation

by

ARTUR JULIUSZ LEWINSKI KOMINCZ

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2006

Major Subject: Electrical Engineering

HIGH FREQUENCY AND HIGH DYNAMIC RANGE

CONTINUOUS TIME FILTERS

A Dissertation

by

ARTUR JULIUSZ LEWINSKI KOMINCZ

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Approved by:

Chair of Committee,	Jose Silva Martinez
Committee Members,	Edgar Sanchez Sinencio
	Frederick Strieter
	Wayne Lepori
Head of Department,	Costas Georghiades

May 2006

Major Subject: Electrical Engineering

ABSTRACT

High Frequency and High Dynamic Range

Continuous Time Filters. (May 2006)

Artur Juliusz Lewinski Komincz,

B.S., Instituto Tecnologico de Queretaro, Mexico

Chair of Advisory Committee: Dr. Jose Silva Martinez

Many modern communication systems use orthogonal frequency division multiplexing (OFDM) and discrete multi-tone (DMT) as modulation schemes where high data rates are transmitted over a wide frequency band in multiple orthogonal sub-carriers. Due to the many advantages, such as flexibility, good noise immunity and the ability to be optimized for medium conditions, the use of DMT and OFDM can be found in digital video broadcasting, local area wireless network (IEEE 802.11a), asymmetric digital subscriber line (ADSL), very high bit rate DSL (VDSL) and power line communications (PLC). However, a major challenge is the design of the analog front-end; for these systems a large dynamic range is required due to the significant peak to average ratio of the resulting signals. In receivers, very demanding high-performance analog filters are typically used to block interferers and provide anti-aliasing before the subsequent analog to digital conversion stage.

For frequencies higher than 10MHz, Gm-C filter implementations are generally preferred due to the more efficient operation of wide-band operational transconductance amplifiers (OTA). Nevertheless, the inherent low-linearity of open-loop operated OTA limits the dynamic range. In this dissertation, three different proposed OTA linearity enhancement techniques for the design of high frequency and high dynamic range are presented. The techniques are applied to two filter implementations: a 20MHz second order tunable filter and a 30MHz fifth order elliptical low-pass filter. Simulation and experimental results show a spurious free dynamic range (SFDR) of 65dB with a power consumption of 85mW. In a figure of merit where SFDR is normalized to the power consumption, this filter is 6dB above the trend-line of recently reported continuous time filters.

To my wife Isabel,

my parents Juliusz and Grazyna

and my brother Pawel.

ACKNOWLEDGMENTS

This work would not have been possible without the support and help of many people; my appreciation goes out to the following:

First, I would like to thank my advisor and committee chair, Dr. Jose Silva, for his outstanding guidance and knowledge during the course of this research. Also, thanks to all my committee members, Dr. Edgar Sanchez Sinencio, Dr. Frederick Strieter and Dr. Wayne Lepori for their great support and attention. It was an honor to work with all of them.

During the course of my Ph.D., the best thing happened to me: I married the love of my life, Isabel. Through good or hard times, she was always cheering me on and bringing joy to my life. There are no words to express my appreciation for that. I love her very much.

I want to give special thanks to Dr. Rainer Fink, for whom I had the opportunity to work in a remarkable and enjoyable project. Not only has he been a great supervisor and professor, but also a good friend who was always there to listen and advise.

Many thanks to my friends and former roommates David and Alberto; we shared together the glory and pain of graduate work, and we learned a lot from each other. To my friends Ari, Marcia, Pedro, Marta, Antonio and Adriana, thank you for your good advice, and for your kind help in times of need.

To Chinmaya, Faisal, Chava, Didem, Feyza, Sebastian, Peyman, Alexander, Hezam, Ranga, Rhadika, Alejandro, Wennie, Julio, Rida, Ahmed, Reza, Sathya, Taner,

Abraham, John, Lorena, Felipe, Gavillero, Pankaj, Sualp, Devrim, Fikret, Elvis, Itza; thanks for great shared moments.

I also want to thank my father for inspiring me to do this, and my mother for always believing in me. Thanks also to my wife's parents for their constant support.

Many thanks go to Mrs. Cook, Nancy and Angela at Sponsored Student Services and Tammy, Jeannie and Ella at the Department of Electrical Engineering for their assistance.

Finally, I want to thank CONACYT for the invaluable financial support that made the achievement of this degree possible.

TABLE OF CONTENTS

Page

Page

LIST OF FIGURES

Page

Page

Page

Page

LIST OF TABLES

Page

1. INTRODUCTION

1.1 The need of analog filters

With low-power and small integrated circuits based on microprocessors, microcontrollers and digital signal processors (DSP), much of the electrical functionality previously implemented with analog electronics, is now efficiently done with digital circuits. This rapid grow in digital electronics deluded to a common misconception that electronic circuits known as “analog” are eventually going to disappear. However, in order to acquire and generate natural signals such as audio, video, radio waves and many others, the need of an analog to digital and digital to analog interfaces remains a must.

Before an analog signal enters the analog to digital converter (ADC), it must be preprocessed by analog continuous time filters (CTF) or a combination between continuous time filters (CTF) and switched capacitors. The CTF serves two main purposes: i) it rejects unwanted frequency signals to avoid overloading the ADC and ii) prevents aliasing by attenuating components with higher frequency components.

Figure 1.1 shows a typical signal in time domain where the amplitude is larger than the input range of the ADC marked with dashed lines. This signal may contain media noise, adjacent frequency channels not intended to be used by the end user, a DC signal, etc. A band-pass filter removes the undesired information, maintaining in-band information

---

This dissertation follows the style of the *IEEE Circuits and Systems II* Journal.

intended for the application. An alternative to the use of analog filters is the removal of out of band signals using digital processing after the ADC, but a larger requirement in the number of bits would be necessary. For example, it has been shown in [1] that the additional necessary number of bits (N) of an ADC to accommodate out of band signals is:

$$N = \frac{Int\left(\frac{I}{S} + 3\right)}{6dB} \qquad (1.1)$$

where I is the power (in dB) of the out of band signals and S is the power of the data to be captured. (Int stands for the integer function) Without the filter, an additional number of bits would complicate the ADC implementation.

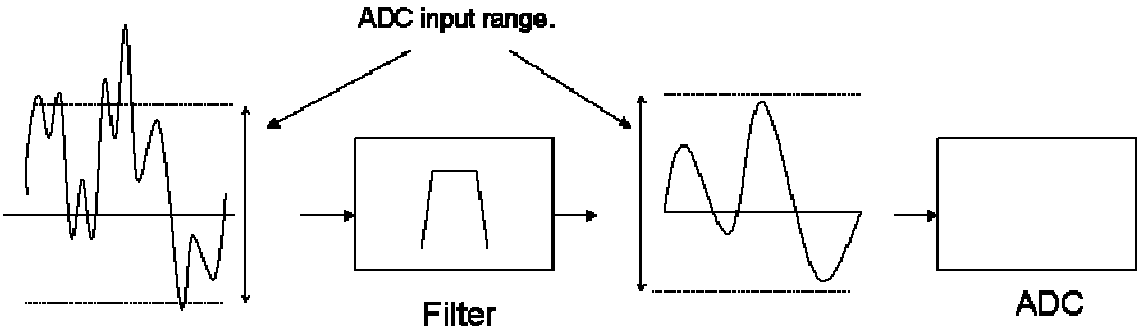


Fig. 1.1 The use of filters to reduce the input range of an ADC.

Whenever a continuous signal is sampled, all the frequencies above half the sampling rate are aliased back to the band of interest; this effect is known as aliasing . Figure 1.2 shows the frequency spectrum of a signal with higher frequency components higher than the half of the sampling rate of the ADC. Once the entire signal is sampled,

the undesired frequency components are aliased back into low frequency, tampering the useful data. To avoid this effect, a low-pass filter is necessary to remove higher frequency components.

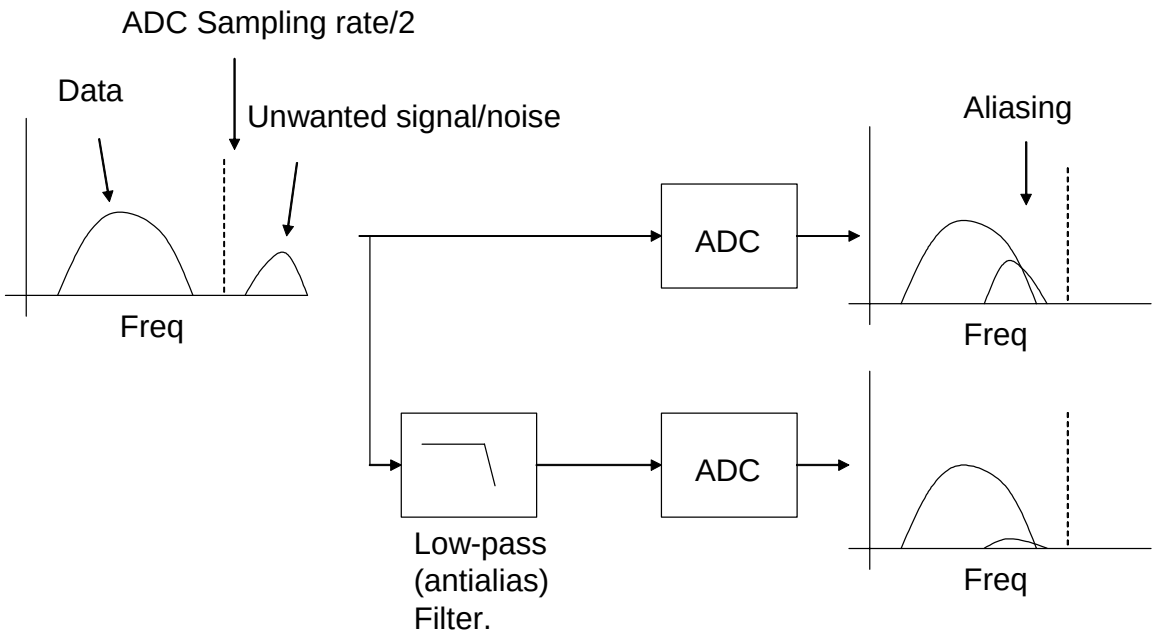


Fig. 1.2. The use of filters to avoid the aliasing problem.

Although there is interest in developing powerful ADCs to remove analog filters and other analog blocks, technological limitations prevent this from being possible [2]. For low frequency operations, high resolutions can be achieved but as frequency increases higher power consumption designs are required to deal with parasitic capacitances that introduce bandwidth limitation; mismatch is also a limiting factor to the accuracy of an ADC. Digital to analog interfaces, also require continuous time

analog filters at the end of the signal path to smoothen the output generated by the digital to analog converter (DAC).

Figure 1.3 shows a block diagram of a typical modern communication system used in wired applications: a DSL modem. In the receive path, the incoming signal, which is weak due to attenuation in the cable, is amplified by a programmable gain amplifier (PGA1). A continuous time filter passes the required range of frequency spectrum while attenuating the out of band information and minimizing the alias signals for the subsequent analog to digital conversion. A second programmable gain amplifier (PGA2) may be used to further adjust the level of the signal to meet the input range of the analog to digital converter (ADC). The signal is then demodulated in the digital domain by the digital signal processor (DSP) and sent out to the user.

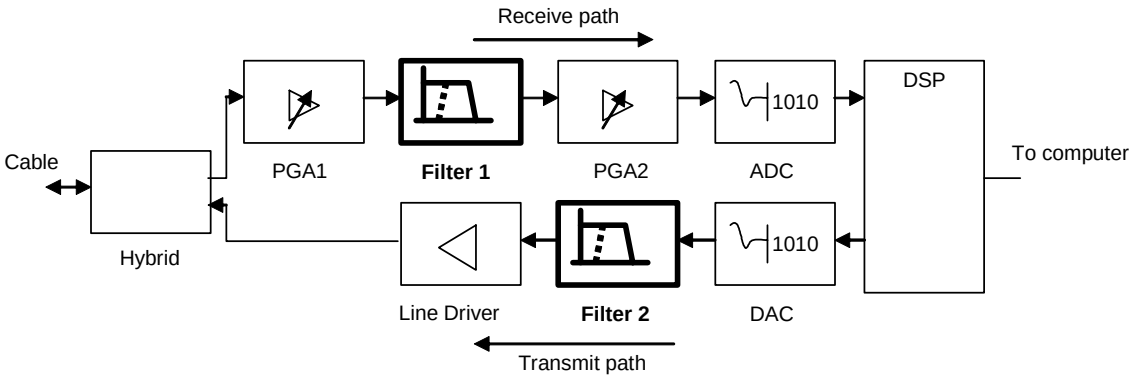


Fig. 1.3. Simplified schematic of a DSL modem.

In the transmit path, the digital data to be sent through the cable is modulated and converted to an analog signal by the use of a digital to analog converter (DAC). The

continuous time filter smoothes the pulse-shaped analog DAC output. Finally, a line driver sends the signal through the cable.

1.2 Challenges in continuous-time filters

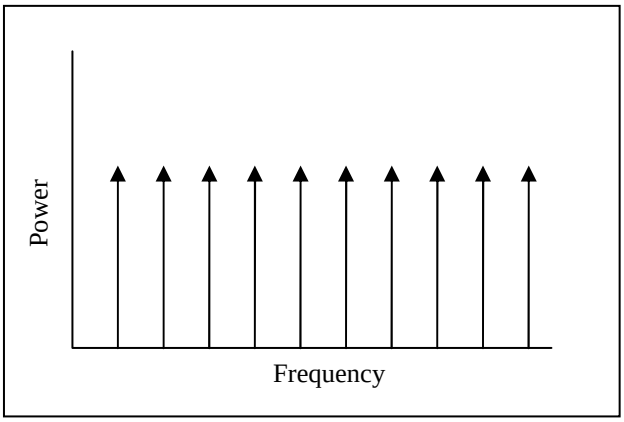
The first filters that used resistors, inductors and capacitors are commonly known as RLC filters. These passive components occupied a very large area, especially at audio frequencies where heavy coils and big capacitors were the most noticeable components in the circuit board. Other applications, such as frequency division multiplexing telephone systems, required cheaper and smaller implementations. This gave rise to miniaturized piezoelectric technologies such as mechanical and crystal filters. Another similar technology based on acoustic waves, is the Surface Acoustic Wave (SAW) filter which is widely used in today's wireless communication circuits. A detailed description of the previous mentioned filters can be found in [3].

Since the invention of the integrated circuit in 1958, more and more external circuitry was merged into a single chip and, as the resolution of integration increases, the concept of having an entire system on a chip (SoC) became possible. Circuit blocks such as the microcontroller, digital signal processor, analog to digital converters and filters can be now integrated into a single chip resulting in cost savings, space reduction and simple interface. Thanks to these features, it is possible to have affordable compact cell phones, miniaturized biomedical implants, portable computers and many other devices.

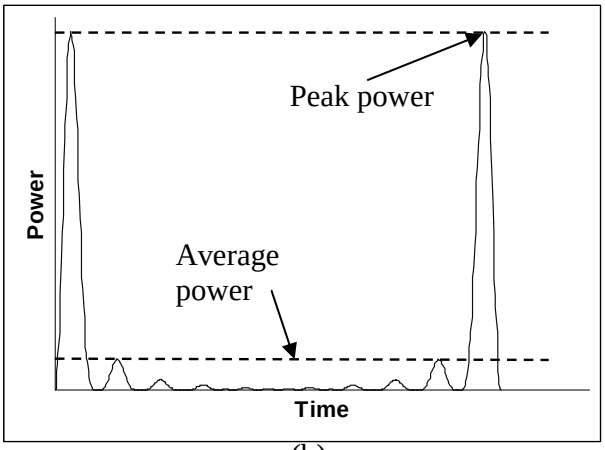
Although feasible, the integration of continuous time filters presents several problems. The integration of inductors in a small semiconductor die is not possible for frequencies lower than several hundreds for megahertz due to very large area requirements and the considerable resistivity of metal layers used to build an inductor. Therefore, active elements based on transistors have to be used to emulate inductors to implement equivalent transfer functions. Unfortunately, active elements introduce additional noise, harmonic distortion components and consume static power. Another problem is that integrated capacitors, resistors and active elements are sensitive to temperature and process parameters variations which affect the selectivity and precision of the filter.

The aforementioned disadvantages present a stringent challenge for many modern communication systems. Actually, integrated continuous time filters have been referred by some authors as “the bottleneck” of communication circuits [4]. This is especially the case of systems using orthogonal frequency division multiplexing (OFDM) and discrete multi-tone (DMT) as modulation schemes. In these schemes, high data rates are transmitted over a wide frequency band in multiple orthogonal sub-carriers. Due to its many advantages such as flexibility, good noise immunity and the ability to be optimized for medium conditions [5],[6] its use can be found in wireless and wireline applications: Digital video broadcasting, local area wireless network (IEEE 802.11a), Asymmetric Digital Subscriber Line (ADSL), Very High Bit Rate DSL (VDSL) and Power Line Communications (PLC). However, the large peak to average ratio of these signals is a design issue [7].

Figure 1.4 shows a typical OFDM signal in frequency and time domain. Figure 1.4(a) shows the signal in frequency domain with ten subcarriers equally spaced. In time domain, (figure 1.4(b)) the signal contains big peaks that occur at the moment when the maximums of all subcarriers coincide in time. Although the average power is small, the input range of the filter has to be large enough in order to accommodate these large peaks.



(a)



(b)

Fig. 1.4. OFDM signal in a) frequency domain and b) time domain.

Figure 1.5 shows an OFDM spectrum with a weak sub-carrier before and after being passed through an active non-linear filter. The non-linearities of the filter causes the big sub-carriers to modulate between each other causing intermodulation components that interfere with neighboring sub-carriers. Thus, intermodulation components act as noisy interferers.

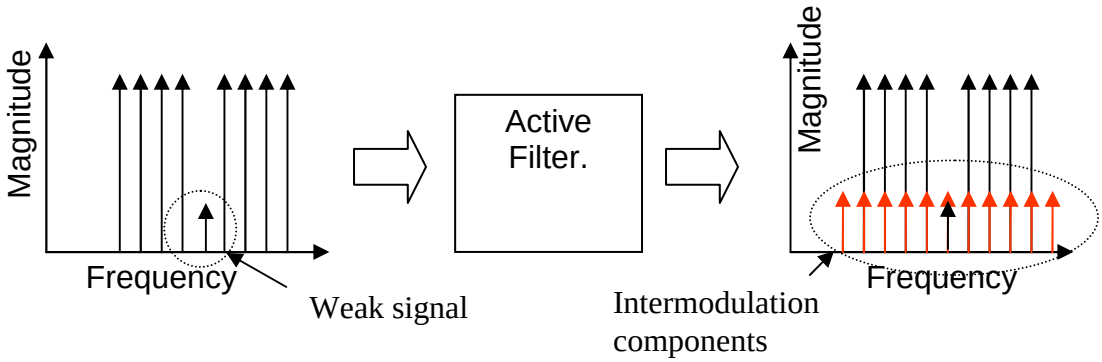


Fig. 1.5 Intermodulation components caused by the distortion of the filter.

The power of the signal divided by the power of the noise, is commonly referred as the Signal to Noise Ratio (SNR). Larger signals permit better SNR but it must be measured within the range such that the distortion of the filter does not generate enough intermodulation components to damage the information contained in the signal. The highest level of the signal divided by the power of noise is the Dynamic Range (DR).

To understand why DR is important, one may simply consider the analogy of a conversation in a noisy room, where the listener may misunderstand or not get some information from the speaker. A larger DR means that either the speaker may talk

loudly or there is less noisy conversation or traffic around improving the clarity of the information. The same happens for communication systems where the information received is corrupted due to the noise generated by the media or electronic devices. Fortunately, communication systems contain error detection algorithms that reply to the transmitter inquiring the repetition of a damaged packet of information. However, the repetition of information degrades the speed of transmission, something that is not desirable in applications given the rapid advancing trend for higher data rates.

In many current and future generation applications, a high DR requirement forces to use external filters such as RLC or SAW. If off-chip solutions are used, besides the higher cost and larger area, internal buffers are also necessary to drive the low impedance usually found in this type of filters as well as the parasitic capacitances and inductances present in the bounding wires and pads. All these factors present a motivation for the search and improvement of the dynamic range of integrated continuous time filters.

As for the problem of temperature and process variations that modify the characteristics of integrated filters, on-chip self-tuning circuits have to be used. The function of this additional circuit is to calibrate the filter to exhibit a desired frequency response. There are many issues in the implementation of this circuit, especially at high frequencies [8].

1.3 State of the art in continuous time filters

Low and medium frequency active filters can be categorized depending of its basic building block implementation. The most popular building blocks are the Operational Amplifier (OP-AMP) and Operational Transconductance Amplifier (OTA).

Ideally, an OP-AMP is a voltage controlled voltage source with infinite gain but in practice the gain of the OP-AMP is finite and decreases for higher frequencies due to internal parasitic capacitances. The linearity of OP-AMPs is excellent for low-frequency applications, however the low gain at high frequencies may not effectively limit the non-linearities. Furthermore, since OP-AMPs work in a closed-loop fashion, they are prone to be unstable which complicates the design for high performance.

Operational transconductance amplifiers (OTA) or simply “transconductors” are voltage controlled current sources. Since a simple transistor is inherently a voltage to current converter; the implementation of OTAs is simpler than OP-AMPs. In most cases, an OTA can be considered as an unbuffered OP-AMP.

Since the internal nodes of an OTA are mostly low-impedance, the bandwidth of operation is quite large allowing its use for high frequencies. The OTA operates in open loop without any local feed-back path and not raising stability problems as in the case of OP-AMPs. However, the non-linear behavior of transistors introduce distortion and a large number of techniques to deal with this problem have been reported in the literature.

To have a general panorama of today’s state of art in active continuous-time filters, the most recent breakthroughs reported in the literature are evaluated. To this end, a figure of merit can be defined. A parameter that considers both SNR and linearity, is

the spurious free dynamic range (SFDR) [9]. SFDR is defined as the dynamic range for an input voltage, such that the power of the harmonic distortion components is equal to the noise power.

The figure of merit consists of the SFDR normalized to the power consumption of a filter per pole in mW:

$$FoM = SFDR - 10\log(P / n_p) \qquad (1.2)$$

The FoM does not consider other parameters such as the quality factors (Q) or other additional features that a reported filter may have, but it gives an indication of the trend of this technology. Figure 1.6 shows FoM vs. frequency of operation for the most recent journal filter publications [10]-[24]. There is a decaying trend line as frequency increases because there is more integrated thermal noise and many linearity techniques cannot be applied for higher frequencies efficiently. The dynamic range depends on the frequency of operation; also reported linearization techniques are not very effective at higher frequencies.

It is interesting to see that most of the reported high frequency techniques use OTAs. This is due to the fact that OTA-C implementations are simpler for frequencies of tenths of MHz and more reliable in terms of stability if compared to Active-RC.

Arising technologies require higher circuit performances and this is the case for analog interfaces requiring continuous time filters. For instance, in ADSL (Asymmetrical Digital Subscriber Lines) cable modem applications, the linearity has to be better than 60dB [25]-[26] and video applications require at least 60 dB of linearity

at 5 MHz [27]. Future trends pushing towards higher data transfers will require higher frequency ranges with equal or better linearity.

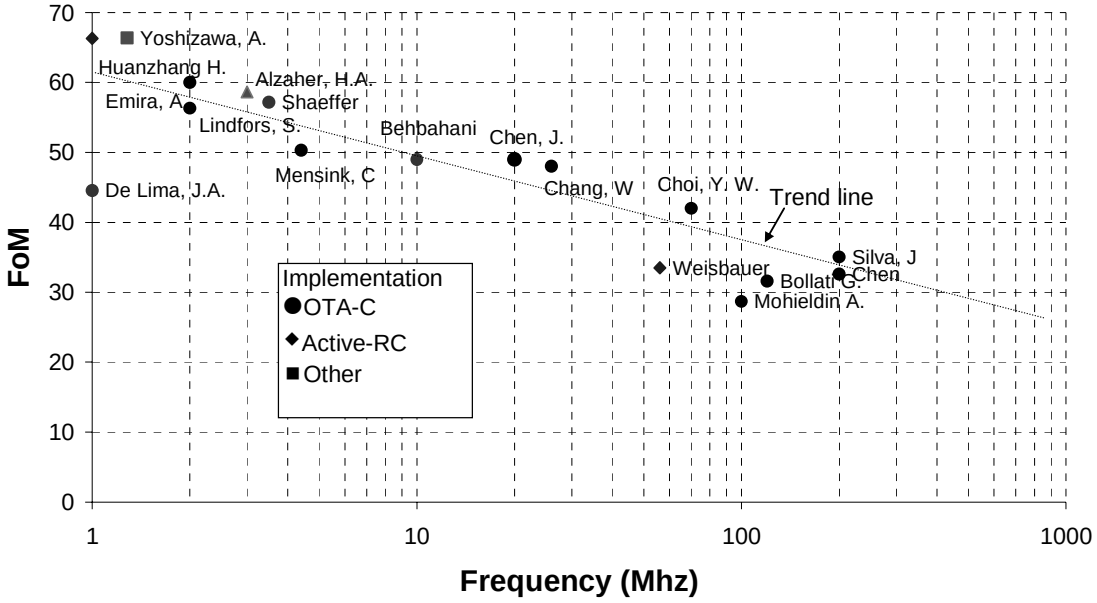


Fig. 1.6 Figure of merit of recent publications about filters.

1.4 Contributions

In this dissertation, three techniques for the design of high dynamic range OTA-C filters are proposed. These techniques are based in the linearization of the most important contributor to the distortion in the OTA: The differential pair.

First, the double differential pair is introduced where the distortion due to one differential pair is cancelled by the auxiliary circuit. If properly dimensioned and biased, the double differential pair offers an advantage of more than 10dB of linearity for the same power consumption and transconductance compared to the typical differential pair

with a very small noise 1-2dB increase. An OTA based on the double differential is presented featuring 25% continuous transconductance tuning with minimal linearity degradation. The OTA is tested in a 20-MHz second order low-pass ladder filter prototype. With a 10.5mW of power per OTA, the filter achieves -65dB IM3 for 1.3Vpp.

The second proposed technique is a triple differential pair architecture. it offers a more robust linearity cancellation with the drawback of reduced transconductance per power. Experimental results for an OTA fabricated in the TSMC 0.35μm CMOS process are presented and compared with recently reported topologies. Draining 2.8mA from a single supply voltage of 3.3V, the transconductor achieves IM3<-70dB for a two-tone input signal of 1.3Vpp measured at 70 MHz. The input referred noise density is only 7nV/√Hz, leading to a SNR of 75dB.

Finally, the non-linear source degeneration differential pair is presented. The linearity of a typical source degenerated structure is improved by more than 10 dB while the overall small signal transconductance is reduced by less than 10%; the additional power needed by the auxiliary circuitry is less than 10 % of the OTA's power, and the noise level increases by no more than 1 dB. A self-bias circuit is used to match the transconductance to polysilicon resistor values serving two purposes: i) ensuring the linearity of the OTA against process parameter variations and ii) allowing the use of polysilicon resistors for filter's terminations. The technique is tested in a 30MHz 5th order elliptic filter consuming 85mW of static power and achieving a spurious free dynamic range (SFDR) of 65dB. With these results, this filter is 6dB above the trend

line shown in figure 1.6. An automatic frequency tuning circuit to is included to reduce the low-pass frequency cut-off with process parameter variations.

1.5 Organization

Section 2 starts by describing the main noise and linearity issues of a simple differential pair. Then, the double differential pair is introduced and studied. A full OTA design using the double differential is described and incorporated in a second order 20-MHz low-pass filter. Simulated and experimental results are included. Finally, the triple differential pair is analyzed. Simulation and experimental results are shown and are compared with previously reported topologies.

Section 3 discusses the non-linear source degeneration technique. A 30-MHz elliptic low-pass filter design is presented suitable for next generation Power Line Communication Systems. Details of the OTA, filter tuning, automatic bias and other issues are addressed. The design of an automatic tuning circuit is explained. Experimental results are shown and compared with previous publications. Finally, section 4 presents the conclusions and summarizes the contributions of this work.

2. LINEARITY ENHANCEMENT TECHNIQUES BASED ON NON-LINEARITY CANCELLATION

Distortion occurs in the voltage to current conversion due to the non-linear behavior of transistors in the differential pair. The first part of this section addresses the linearity and noise issues of the differential pair. Then, the techniques based on non-linearity cancellation are presented: The double differential pair and the triple differential pair. The double differential pair is discussed and an OTA and filter implementation is presented. The last part of the section discusses the triple differential pair and describes simulation and experimental results.

2.1 The differential pair

The differential pair is the most popular structure used in the implementation of differential OTAs (Figure 2.1). One of the more important properties of the differential pair is that it has a very good rejection to common mode signals; however the linearity is limited due to the tail current transistor. In this subsection the analysis of distortion and noise of the differential pair is presented. The outcomes are used as the basis for the evaluation of the proposed techniques.

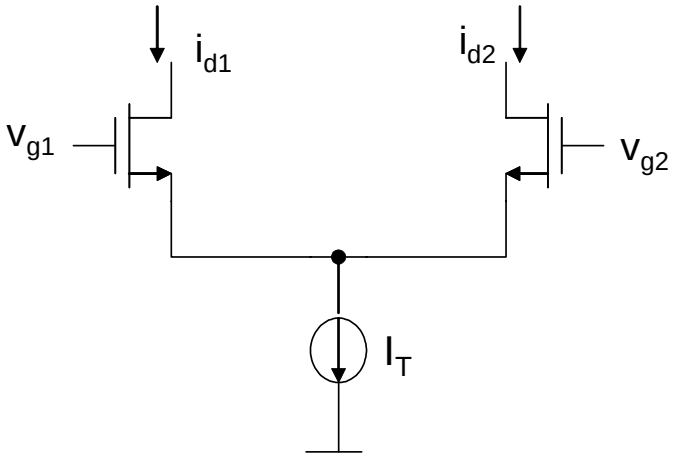


Fig. 2.1. The differential pair.

2.1.1 Distortion

For a MOS transistor working in saturation, the drain current is given by:

$$i_d = K(v_g - v_s - V_T)^2 \qquad (2.1)$$

where V_T is the threshold voltage and K is a physical constant given by:

$$K = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right) \qquad (2.2)$$

W and L are the width and length of the transistor respectively; μ is the mobility of carriers (electrons for N-type transistors and holes for P-type transistors) and C_{ox} is the oxide capacitance per unit area.

For the differential pair shown in fig. 2.1, the input voltage of each transistor is:

$$v_{g1} = v_{cm} + \frac{v_{in}}{2}$$
$$v_{g2} = v_{cm} - \frac{v_{in}}{2} \qquad (2.3)$$

where v_{cm} is the common mode voltage and v_{in} the differential input voltage. Defining $v_c=v_{cm}-v_s-V_T$ and using (2.2), $i_{d1}-i_{d2}$ is given by:

$$i_{d1} - i_{d2} = -2Kv_{in}v_c \quad (2.4)$$

Due to the current source, the sum of i_{d1} and i_{d2} must be equal to I_T, then:

$$i_{d1} + i_{d2} = I_T = 2K\left(\frac{v_{in}^2}{4} + v_c^2\right) \quad (2.5)$$

Solving for v_c in (2.5) and using the outcome in (2.4) yields:

$$i_{d1} - i_{d2} = 2Kv_{in}\sqrt{\frac{I_T}{2K} - \frac{v_{in}^2}{4}} \quad (2.6)$$

Defining differential current as $i_o=(i_{d1}-i_{d2})/2$, (2.6) can be expressed as:

$$i_o = \frac{g_m v_{in}}{2}\sqrt{1 - \frac{v_{in}^2}{4V_{dssat}^2}} \quad (2.7)$$

where g_m is the transconductance of the transistor given by:

$$g_m = 2KV_{dssat} \quad (2.8)$$

and V_{dssat} is the DC saturation voltage given by:

$$V_{dssat} = V_G - V_S - V_T = \sqrt{\frac{I_T}{K}} \quad (2.9)$$

For a simplified distortion analysis, the above expression can be expanded in taylor series around $v_{in}=0$, such that:

$$i_o = \sum_{n=0} G_{M(2n+1)} \cdot v_{in}^{2n+1} \quad (2.10)$$

where,

$$G_{Mj} = \frac{g_m}{2^{2(j-1)} V_{dssat}{}^{j-1}} \qquad (2.11)$$

G_{M1} is the linear coefficient and G_{M3},G_{M5},… are undesired non-linear terms.. For weak signals, the distortion is mainly produced by the third order term; therefore higher terms can be ignored leading to:

$$i_o \approx G_{m1} v_{in} + G_{m3} v_{in}{}^3 \qquad (2.12)$$

The linearity can be measured in terms of intermodulation distortion. Two sinusoidal tones are used for the input such that:

$$v_{in} = \frac{A}{2}\cos(\omega_1 t) + \frac{A}{2}\cos(\omega_2 t) \qquad (2.13)$$

where A is maximum amplitude and ω_1 and ω_2 are the angular frequencies of each tone. Using (2.13) in (2.12) and trigonometric identities, one arrives at:

$$\begin{aligned} i_o = & \left(\frac{G_{m1}A}{2} + \frac{9G_{M3}A^3}{32}\right)(\cos(\omega_1 t) + \cos(\omega_2 t)) \\ & + \left(\frac{3G_{M3}A^3}{32}\right)\begin{pmatrix}\cos((2\omega_1 - \omega_2)t) + \cos((2\omega_2 - \omega_1)t) \\ + \cos((2\omega_1 + \omega_2)t) + \cos((2\omega_2 + \omega_1)t)\end{pmatrix} \\ & + \left(\frac{G_{M3}A^3}{32}\right)(\cos(3\omega_1 t) + \cos(3\omega_2 t)) \end{aligned} \qquad (2.14)$$

The second term contains the intermodulation products. Since these components are caused by the third order term in (2.12) it is referred as the third order intermodulation distortion symbolized IM3 and it is measured as the power ratio of one of the intermodulation products to one fundamental tone. Therefore:

$$IM3 = \frac{\frac{3G_{M3}A^3}{32}}{\frac{G_{m1}A}{2} + \frac{9G_{M3}A^3}{32}} \qquad (2.15)$$

Since G_{M3} is usually very small compared to G_{M1}, then:

$$IM3 = \frac{3G_{M3}A^2}{16G_{m1}} \qquad (2.16)$$

Applying (2.11) in (2.16) results in:

$$IM3 = \frac{3A^2}{128V_{dssat}{}^2} \qquad (2.17)$$

According to (2.17), using larger V_{dssat} yields a better linearity. However, in order to keep all the transistors working in saturation, V_{dssat} has to be limited as shown in fig. 2.2 to:

$$V_{dssat1} < (V_{cm} - V_{ss}) - (V_{dsat2} + V_T) \qquad (2.18)$$

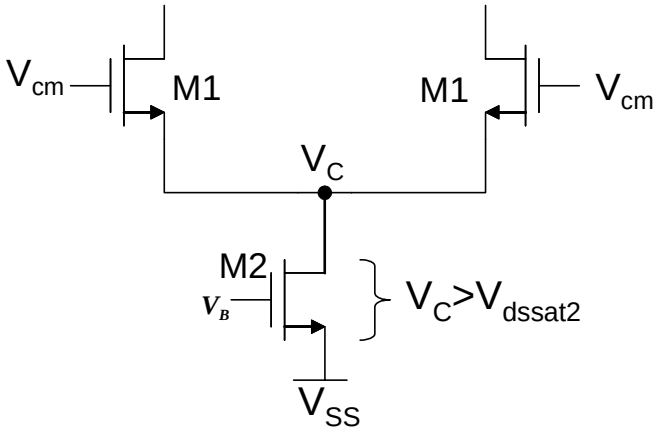


Fig. 2.2. Differential pair with tail current transistor.

To further reduce the distortion, a resistor connected between the sources of transistors M1 and M2 can be used as shown in fig. 2.3. To simplify the analysis, the middle node of the resistor is referred as v_r, then the voltage at the sources of M1 and M2 is.

$$v_{s1} = v_r + \frac{v_{res}}{2} \qquad (2.19)$$

$$v_{s2} = v_r - \frac{v_{res}}{2} \qquad (2.20)$$

where v_{res} is the voltage drop across the resistor. Using (2.1), (2.19) and (2.20) the drain currents are:

$$i_{d1} = K(V_{cm} + \frac{v_{in}}{2} - v_r - \frac{v_{res}}{2} - V_T)^2 \qquad (2.21)$$

$$i_{d2} = K(V_{cm} - \frac{v_{in}}{2} - v_r + \frac{v_{res}}{2} - V_T)^2 \qquad (2.22)$$

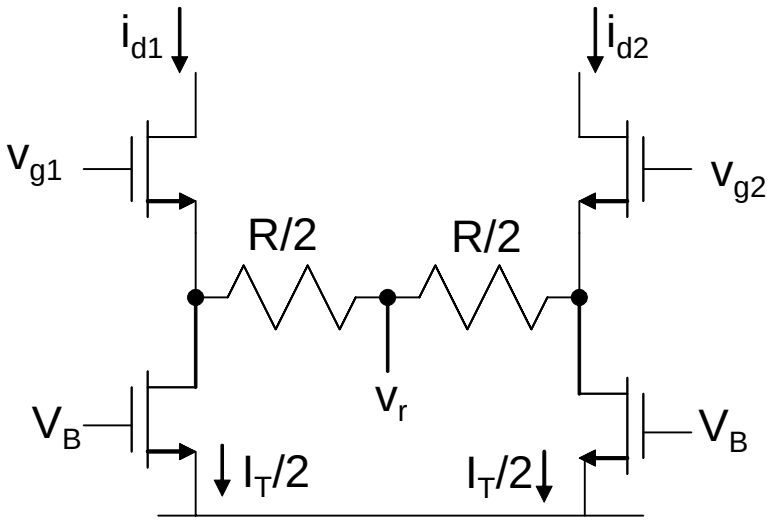


Fig. 2.3. Differential pair with source degeneration.

Defining $vc=V_{cm}-v_r-V_T$, and following the same procedure as (2.4) to (2.7), one arrives at:

$$i_o = \frac{g_m(v_{in}-v_{res})}{2}\sqrt{1-\frac{(v_{in}-v_{res})^2}{4V_{dssat}{}^2}} \quad (2.23)$$

where the taylor expansion is given by:

$$i_o = \sum_{n=0}^{\infty} G_{M(2n+1)} \cdot (v_{in}-v_{res})^{2n+1} \quad (2.24)$$

Notice that the only difference between (2.24) and (2.10) is that v_{res} is subtracted to v_{in}. The current passing through the resistance is $i_{res}= i_{d1}-I_T/2 = -(i_{d2}-I_T/2)$; Clearing I_T yields,

$$i_{res} = \frac{i_{d1}-i_{d2}}{2} = i_o \quad (2.25)$$

Then the voltage across the resistance is:

$$v_{res} = i_o R \quad (2.26)$$

If (2.26) is used in (2.23), a fourth order equation would result that can be very complex and tedious to solve i_o in terms of v_{in}. An alternative is to obtain the solution directly in a series expansion which for the purpose of studying the linearity is more useful. The solution in a series expansion can be expressed as:

$$i_o = \sum_{k=0}^{\infty} C_{2k+1} v_{in}{}^{2k+1} \quad (2.27)$$

where C_k are unknown coefficients. To find these, (2.27) can be plugged in (2.24) resulting in:

$$\sum_{k=0}^{\infty} C_{2k+1} v_{in}{}^{2k+1} = \sum_{n=0}^{\infty} G_{M(2n+1)} \cdot (v_{in} - R\sum_{k=0}^{\infty} C_{2k+1} v_{in}{}^{2k+1})^{2n+1} \qquad (2.28)$$

Notice in the right hand expression that terms in the summatory with v_{in} will only be produced when n=0, terms with vin^3 when n=0 and n=1, terms with vin^5 with n=0, n=1 and n=2. Therefore, if we are only interested to solve C_1,C_3 and C_5 we can perform the summatory up to n=2 and k=2 and ignore terms elevated to a power higher than five. Then, (2.28) becomes:

$$\begin{aligned} &C_1 v_{in} + C_3 v_{in}{}^3 + C_5 v_{in}{}^5 = G_{M1}((1 - RC_1)v_{in} - RC_3 v_{in}{}^3 - RC_5 v_{in}{}^5) \\ &+ G_{M3}((1 - RC_1)v_{in} - RC_3 v_{in}{}^3 - RC_5 v_{in}{}^5)^3 \\ &+ G_{M5}((1 - RC_1)v_{in} - RC_3 v_{in}{}^3 - RC_5 v_{in}{}^5)^5 \end{aligned} \qquad (2.29)$$

Expanding and ignoring terms vin with order higher than five yields,

$$\begin{aligned} &\left((1 + G_{M1}R)C_1 - G_{M1}\right)v_{in} + \left(C_3 G_{m1} R + G_{M3}(1 - C_1 R)^3\right)v_{in}{}^3 \\ &+ \left((1 + G_{M1}R)C_5 + 3G_{M3}(1 - RC_1)^2 RC_3 + G_{M5}(1 - RC_1)\right)v_{in}{}^5 = 0 \end{aligned} \qquad (2.30)$$

For this equation to hold, each of the coefficient has to be zero, then it is straightforward to solve C_1, the C_3 and finally C_5, thus:

$$C_1 = \frac{G_{M1}}{(1 + RG_{M1})} \qquad (2.31)$$

$$C_3 = \frac{G_{M3}}{(1 + RG_{M1})^4} \qquad (2.32)$$

$$C_5 = \frac{G_{M5} + R(G_{M1}G_{M5} - 3G_{M3}{}^2)}{(1 + RG_{M1})^7} \qquad (2.33)$$

Finally the output current can be expressed as:

$$i_o = \frac{G_{M1}}{(1+RG_{M1})} v_{in} + \frac{G_{M3}}{(1+RG_{M1})^4} {v_{in}}^3 + \frac{G_{M5} + R(G_{M1}G_{M5} - 3{G_{M3}}^2)}{(1+RG_{M1})^7} {v_{in}}^5 \qquad (2.34)$$

For weak non-linearities, the third term is higher than the fifth order term being the larger contributor to distortion, then using (2.13) in (2.34) results in:

$$IM3 = \frac{3A^2}{128{V_{dssat}}^2(1+N_r)^3} \qquad (2.35)$$

where N_r is the degeneration factor given by $N_r=G_{M1}R$. Higher degeneration factors improve the linearity at the cost of reduced linear transconductance given by:

$$G_M = \frac{G_{M1}}{(1+N_r)} \qquad (2.36)$$

2.1.2 Noise

Figure 2.4 presents the degenerated differential pair with all the equivalent noise sources.

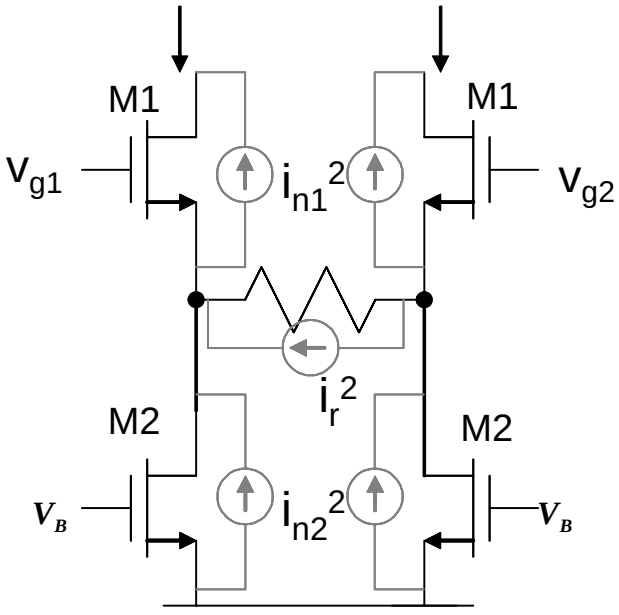


Fig. 2.4. Noise sources in the degenerated differential pair.

Each noise source is given by:

$$\frac{i_{n1}^{\ 2}}{Hz} = 4kT\gamma g_{m1} \qquad (2.37)$$

$$\frac{i_{n2}^{\ 2}}{Hz} = 4kT\gamma g_{m2} \qquad (2.38)$$

$$\frac{i_{r}^{\ 2}}{Hz} = \frac{4kT}{R} \qquad (2.39)$$

where k is the Boltzman constant, T the temperature, γ is typically in the range of 0.7 to 2, g_{m1} and g_{m2} the transconductance of M1 and M2 respectively. The total output noise current can be found as:

$$\frac{i_{no}^{\ 2}}{Hz} = 4kT\left(\frac{2}{(2+g_{m1}R)^2}\gamma g_{m1} + \frac{g_{m1}^{\ 2}R}{(2+g_{m1}R)^2} + 2\frac{(g_{m1}R)^2}{(2+g_{m1}R)^2}\gamma g_{m2} \right) \quad (2.40)$$

Using the definition in (2.11) where $G_{M1}=g_{m1}/2$, yields:

$$\frac{i_{no}^{\ 2}}{Hz} = 4kT\left(\frac{1}{(1+G_{M1}R)^2}\gamma G_{M1} + \frac{G_{m1}^{\ 2}R}{(1+G_{M1}R)^2} + 2\frac{(G_{M1}R)^2}{(1+G_{M1}R)^2}\gamma g_{m2} \right) \quad (2.41)$$

Since $Nr=G_{M1}R$, the input referred noise is:

$$\frac{v_{no}^{\ 2}}{Hz} = \frac{\dfrac{i_{no}^{\ 2}}{Hz}}{\dfrac{G_{m1}^{\ 2}}{(1+N_r)^2}} = \frac{4kT}{G_{m1}}\left(\gamma + N_r + 2N_r^{\ 2}\gamma\frac{g_{m2}}{G_{m1}} \right) \qquad (2.42)$$

The third term inside the parenthesis is due to the noise of the tail current sources. This term can be minimized by reducing g_{m2} with respect to G_{m1}. However, this term can be eliminated if the differential pair is arranged as shown in figure 2.5. Then,

the noise due to the tail current is equally injected to both branches appearing as common-mode rather than differential.

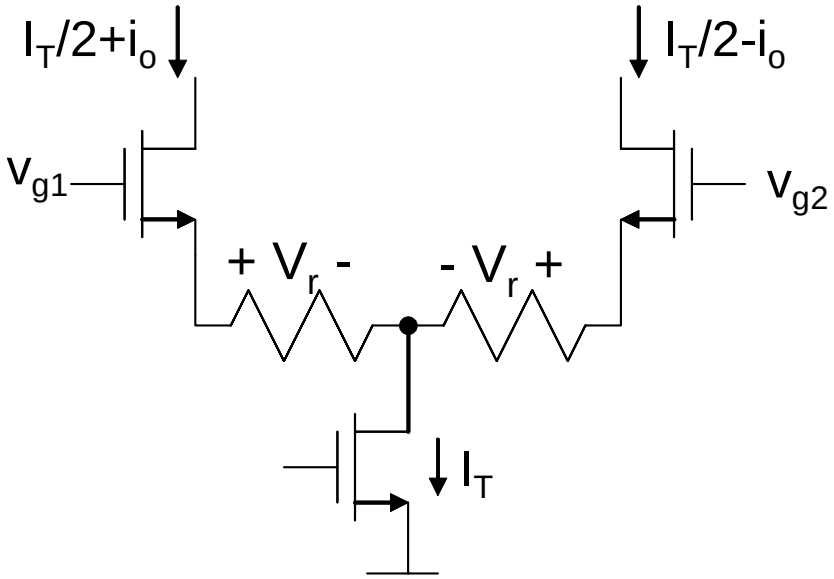


Fig. 2.5. Pseudo-differential pair with the tail current in the middle.

The input referred noise density of the DP of fig. 2.5 is then given by:

$$v_{in}^{\ 2} = \frac{4kT}{G_{m1}}(\gamma + N_r) \quad (2.43)$$

The disadvantage of this topology is that there is a DC voltage drop due to the current I_T passing through the resistors given by:

$$V_r = \frac{I_T R}{4} \qquad (2.44)$$

This voltage drop limits the voltage headroom for Vdsaat1 and Vdssat2 and therefore Nr must be limited.

From the analysis shown here, it can be seen that the distortion can be improved by using larger V_{dssat1} but the supply voltage limits this value. The increase of the degeneration factor (Nr) is then a good alternative for improved linearity but the drawback is that excessive degeneration factors reduce the total transconductance (for the same amount of power) and increase the noise.

2.2 The double differential pair

The double differential pair consists of two differential pairs with cross-coupled outputs such that the third order distortion components are cancelled. The following sub-sections present the analysis and performance comparison with the conventional simple differential pair.

2.2.1 Analysis

Figure 2.6 shows the double differential pair where the total output is given by,

$$i_{oT} = i_{o1} - i_{o2} \quad (2.45)$$

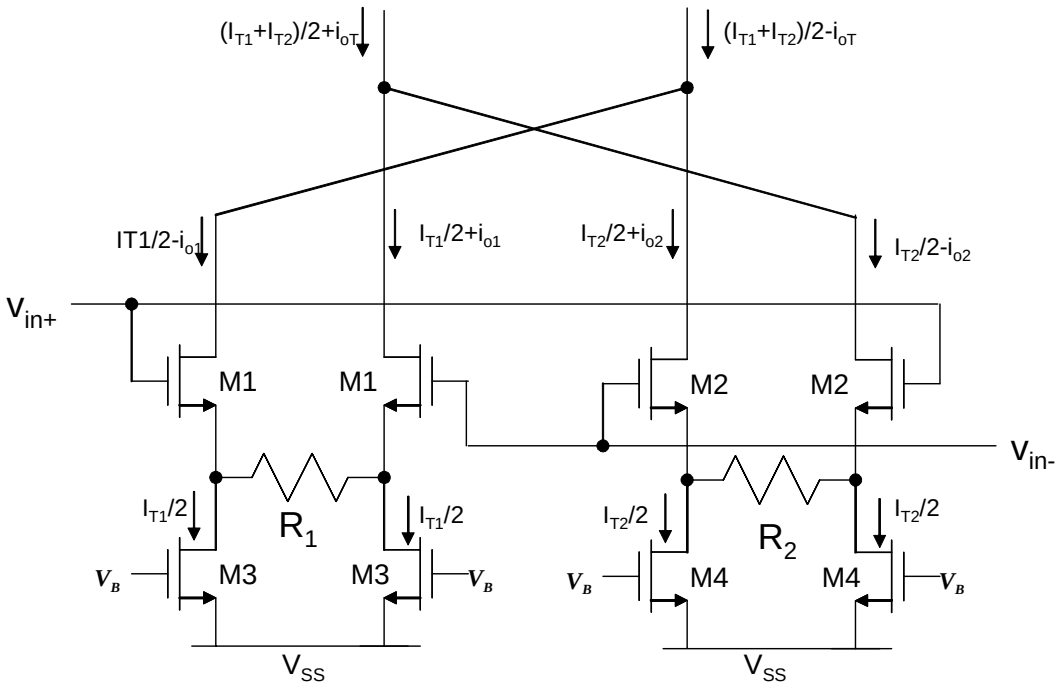


Fig. 2.6. The double differential pair.

Based on (2.34), i_o is then given by (the fifth order component is neglected for simplicity):

$$i_{oT} = \left(\frac{G_{M1,1}}{(N_{r1}+1)} - \frac{G_{M1,2}}{(N_{r2}+1)}\right)v_{in} + \left(\frac{G_{M3,1}}{(N_{r1}+1)^4} - \frac{G_{M3,2}}{(N_{r2}+1)^4}\right)v_{in}{}^3 \qquad (2.46)$$

For cancellation of the third order component, which is the main contribution to distortion component, the following condition has to be met,

$$\frac{G_{M3,1}}{(N_{r1}+1)^4} = \frac{G_{M3,2}}{(N_{r2}+1)^4} \qquad (2.47)$$

Using (2.8) and (2.2), the above expression can be presented as:

$$\frac{I_{T1}}{I_{T2}}\left(\frac{2+\sqrt{I_{T1}K_1}(R_1+R_{\theta 1})}{2+\sqrt{I_{T2}K_2}(R_2+R_{\theta 2})}\right)^8=\left(\frac{(W/L)_1}{(W/L)_2}\right)^3 \qquad (2.48)$$

Equation (2.48) also includes an additional resistance R_θ in series with the degeneration resistance to consider the mobility degradation effect. This effect has an important contribution in the linearity, especially for small channel lengths. The equivalent resistance due to mobility degradations [28] is:

$$R_\theta=\frac{\theta}{\left(\frac{W}{L}\right)\mu_o C_{ox}} \qquad (2.49)$$

where μ_0 is the low-field mobility and θ the mobility constant given by:

$$\theta=\frac{1}{L\cdot E_c}+\theta_T \qquad (2.50)$$

The first term of (2.50) represents the mobility degradation due to the lateral electric field where Ec is the lateral critical electric field. θ_T is a fitting parameter to also consider the mobility due to the transversal electric field. Typical values of θ are in the order of 0.3 V^{-1} to 2 V^{-1} for sub-micron technologies.

To corroborate (2.48), the circuit of fig. 2.6 was simulated using Cadence with the following values: $(W/L)_1$=20μm/1μm, $(W/L)_1$=40μm/1μm, μC_{ox}=120μA/V, R_1=2kΩ and R_2=500Ω. Figure 2.7 shows the IM3 vs. I_{T2} for an input voltage of 200_{mVpp} around 20MHz for three different I_{T1}. A fourth curve depicted with a wide line shows the IM3 of the larger differential pair for reference. Notice that for the three values of I_{T1} there is a I_{T2} at which IM3 is improved by almost 20dB. To verify that (2.48) agrees with simulated results, fig 2.8 shows the relationship between I_{T2} and I_{T1} where the maximum

linearity is achieved. Notice that if mobility degradation is not considered (eg $R_{\theta 1}=R_{\theta 2}=0$), (2.48) significantly deviates from simulated results. This is due to the fact that the term in the parenthesis of the left-hand side of (2.48) is elevated to the power of eight and any small variations, such as the mobility degradation resistance, produce a significant deviation. However, if mobility degradation is considered ($\theta=1.2V^{-1}$), then (2.48) is close to the simulation result.

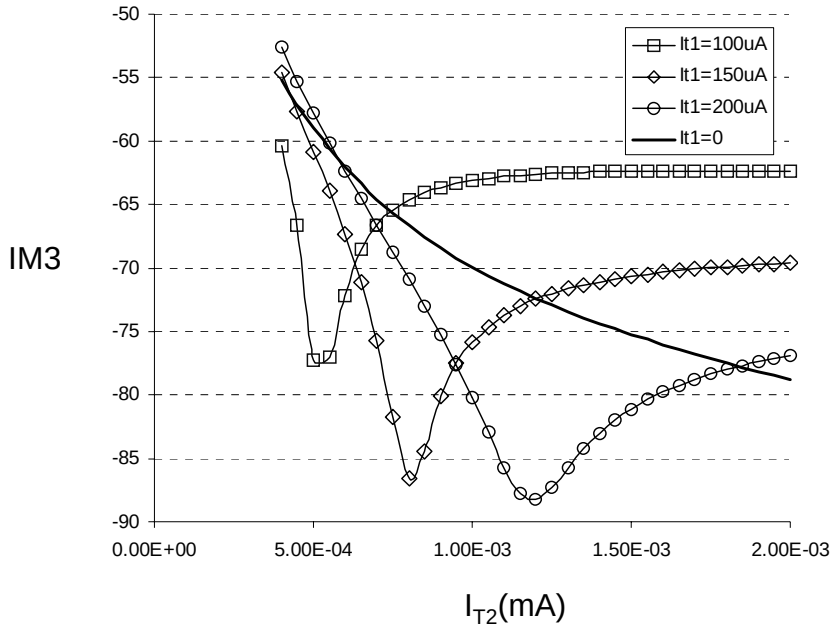


Fig. 2.7. Cadence IM3 simulations for the circuit of figure 2.6.

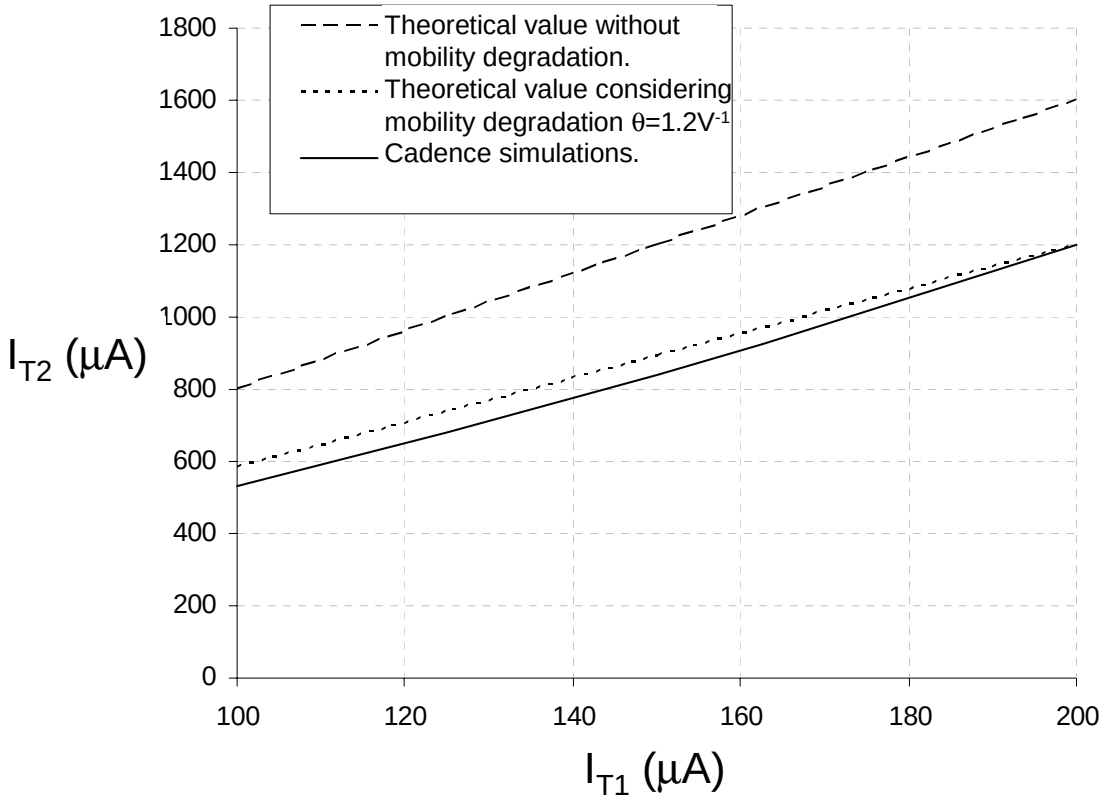


Fig. 2.8. Relation between I_{T1} and I_{T2} for optimal linearity.

As shown in the above analysis, to effectively suppress the third order component, one must consider θ. Similar reported structures that do not consider the mobility degradation effect are subject to large errors and the linearity improvement may not be optimal. Even if considered, the mobility degradation factor θ is a process dependent parameter and cannot be accurately predicted nor controlled.

2.2.2 Improvement comparison

Since the outputs of the differential pairs are subtracted, the effective transonductance G_{mT} of the DDP is reduced by:

$$G_{MT} = \frac{G_{M1,1}}{(N_{r1}+1)} - \frac{G_{M1,2}}{(N_{r2}+1)} \quad (2.51)$$

In addition, the noise increases due to the contribution of both differential pairs and additional current sources. Adding all noise components it can be shown that the input referred noise of the DDP is:

$$\frac{v_{no}^{\ 2}}{Hz} = 4kT \frac{G_{M1}(1+N_{r2})^2\left(\gamma + N_{r1} + 2N_{r1}^{\ 2}\gamma\frac{g_{m3}}{G_{m1}}\right) + G_{M1}(1+N_{r2})^2\left(\gamma + N_{r2} + 2N_{r2}^{\ 2}\gamma\frac{g_{m4}}{G_{m2}}\right)}{G_{M1}^{\ 2}(1+N_{r2})^2 - G_{M2}^{\ 2}(1+N_{r1})^2} \quad (2.52)$$

Although the DDP presents reduced harmonic distortion, the transconductance is decreased and noise increases. Then, it is not clear if there is a real improvement in the overall signal to noise ratio compared to the conventional simple differential pair (SDP). To this end, a simulation was performed to give to compare the DDP and the SDP for the same power consumption and the same transconductance (Fig. 2.9). The SDP is designed to use the same Vdsat as the transistors in the DDP but it uses a larger degeneration factor in order to present equal transconductance.

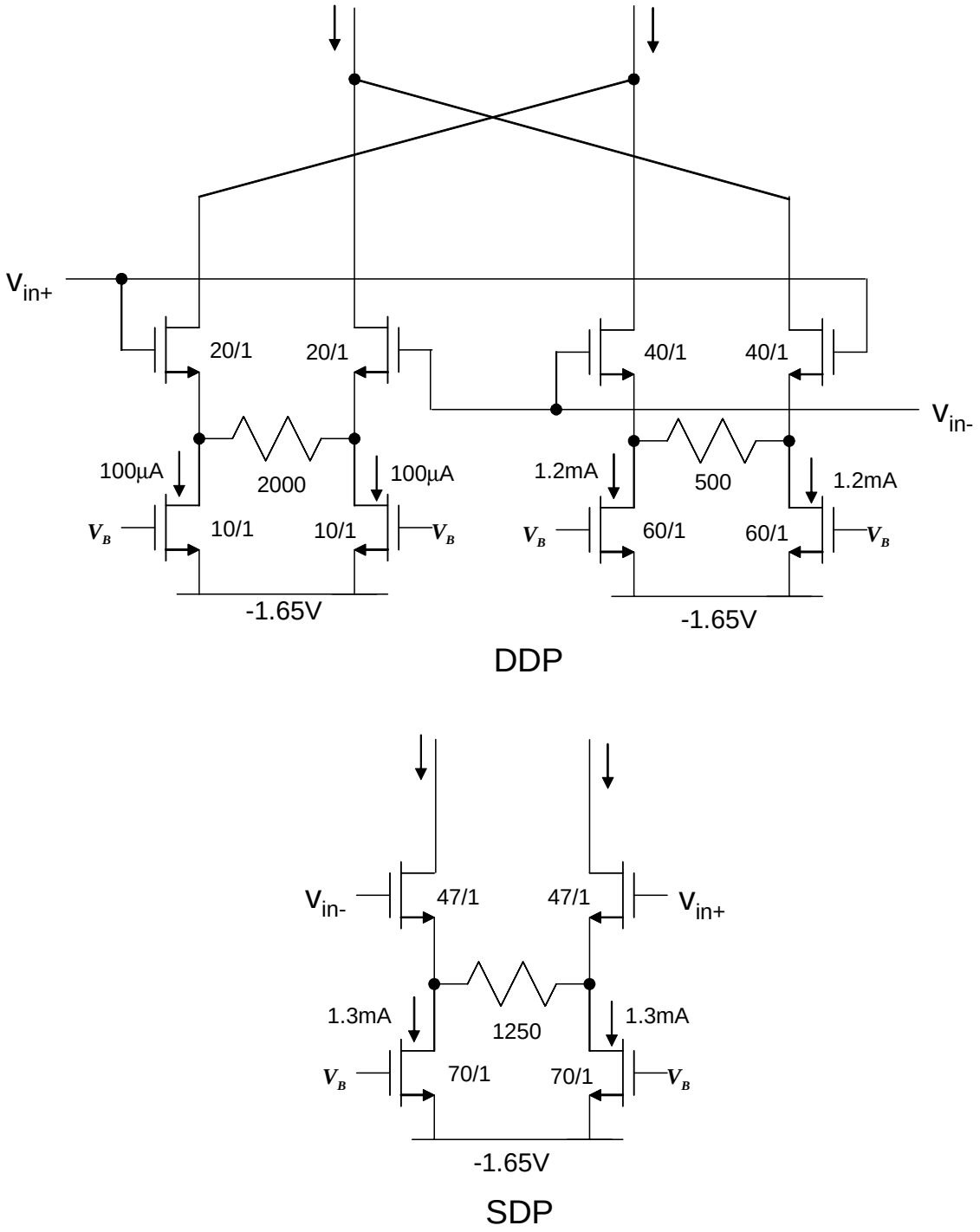


Fig. 2.9. SDP and DDP designs for comparison with same transconductance, Vdsat and power consumption.

Table 2.1 presents the main design parameters for both circuits. The degeneration factor for the SDP is higher by 2.5 times in order to achieve the same transconductance as the SDP. This larger Nr improves the distortion of the SDP but also increases the input referred noise due to the tail current transistors resulting in just a slightly smaller input referred noise density compared to the DDP. The transconductance for both structures is 500μA/V.

Table 2.1. Results for the comparison between SDP and DDP.

Parameter	**SDP**	**DDP**
Degeneration factor	1.75	0.75
Vdsat	350mV	350mV
Input referred noise density	6.8nV/Hz	7.8nV/Hz
Current consumption	1.4mA	1.4mA
Transconductance	500μA/V	500μA/V

Both structures in fig. 2.9 were simulated for different input amplitudes and the IM3 was measured. Fig 2.10 shows a plot of the linearity improvement of the DDP over the SDP ($IM3_{SDP}$-$IM3_{DDP}$) for the same SNR. The SNR was calculated for a bandwidth of 10MHz. Up to 60dB of SNR, the DDP achieves more than 10dB of linearity improvement over the SDP. However as the input signal is larger (In this example SNR>60dB), the linearity improvement worsens due to the fifth order non-linearities caused by the smaller V_{dsat} differential pair used in the DDP.

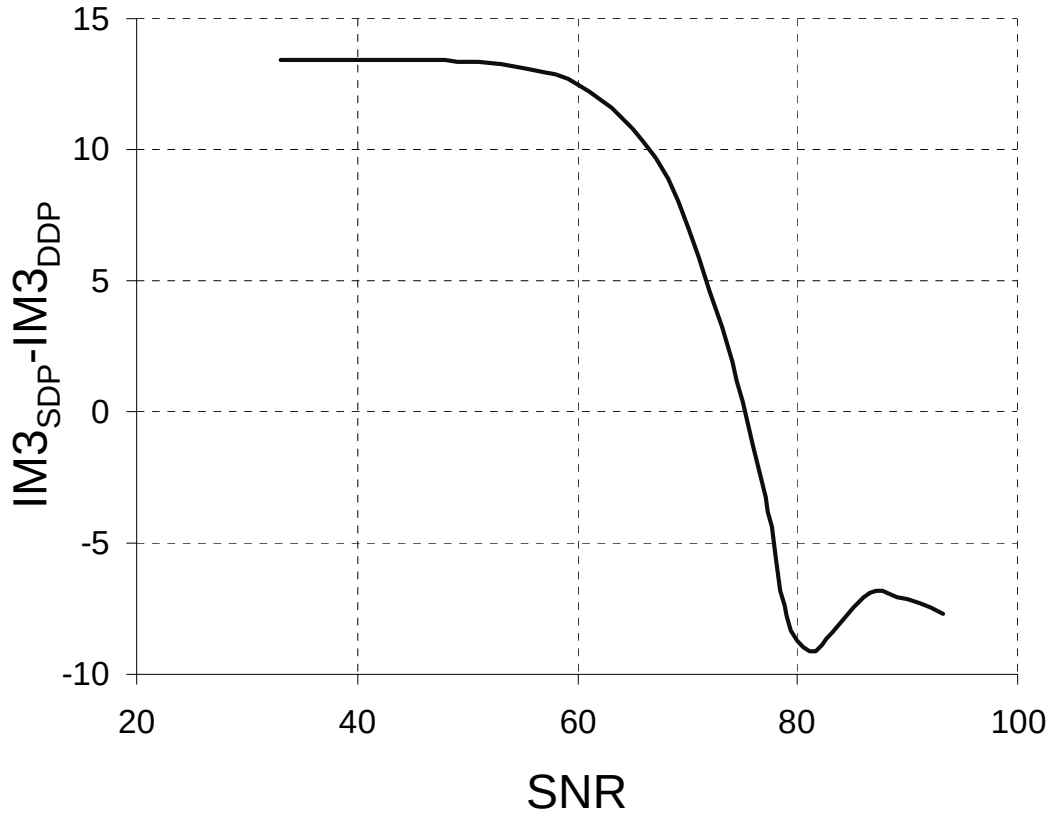


Fig. 2.10. Improvement in IM3 of the DDP over the SDP.

The frequency limits to achieve high linearity are mainly dictated by the decay of degeneration resistance due to effective parasitic capacitances at the source of transistors M1. If Cs is the parasitic capacitance at the source of transistors M1, the frequency limit to hold the linearity is approximately wl=2/(RCs) where R is the degeneration resistor. Figrure 2.11 shows the IM3 plot vs. frequency for the circuit in figure 2.9.

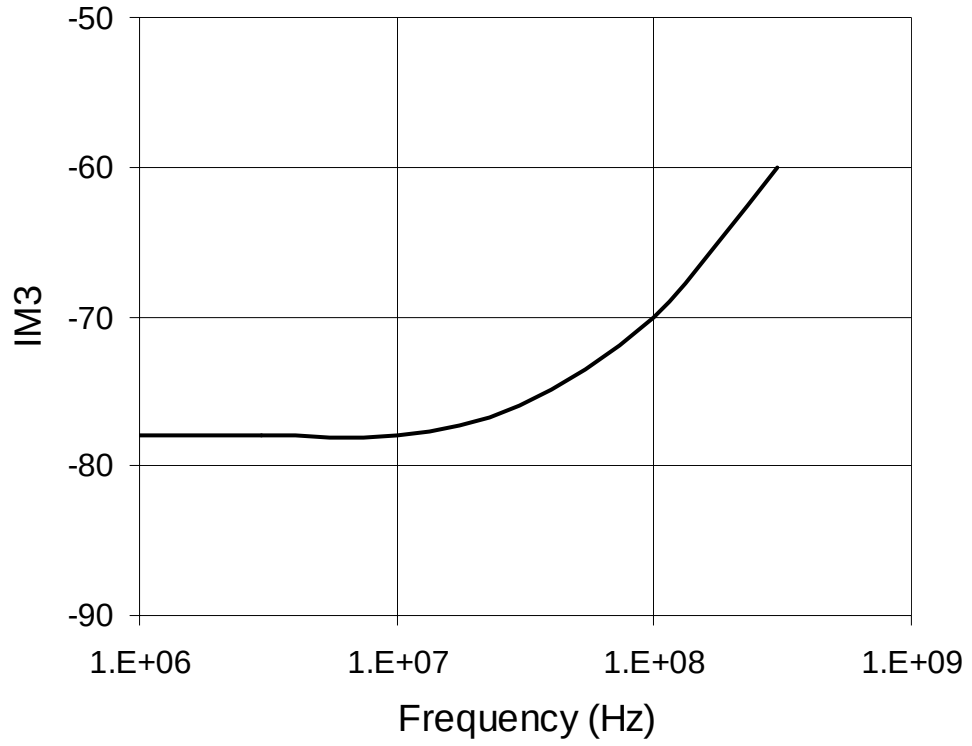


Fig. 2.11 IM3 plot vs. frequency.

2.3 A 20 MHz second order low-pass filter

The double differential technique is used in an OTA-C low-pass filter ladder prototype to verify its application. The following subsections describe the OTA and filter design. At the end of this subsection, experimental results are presented.

2.3.1 OTA design

Figure 2.12 shows the overall OTA design. For the input stage, the double differential pair is used in order to achieve the non-linearity cancellation as described in

the previous section. Transistors M1 and M2 use a V_{dsat} a 280mV and 330mV, respectively, and the degeneration factors are Nr=1.

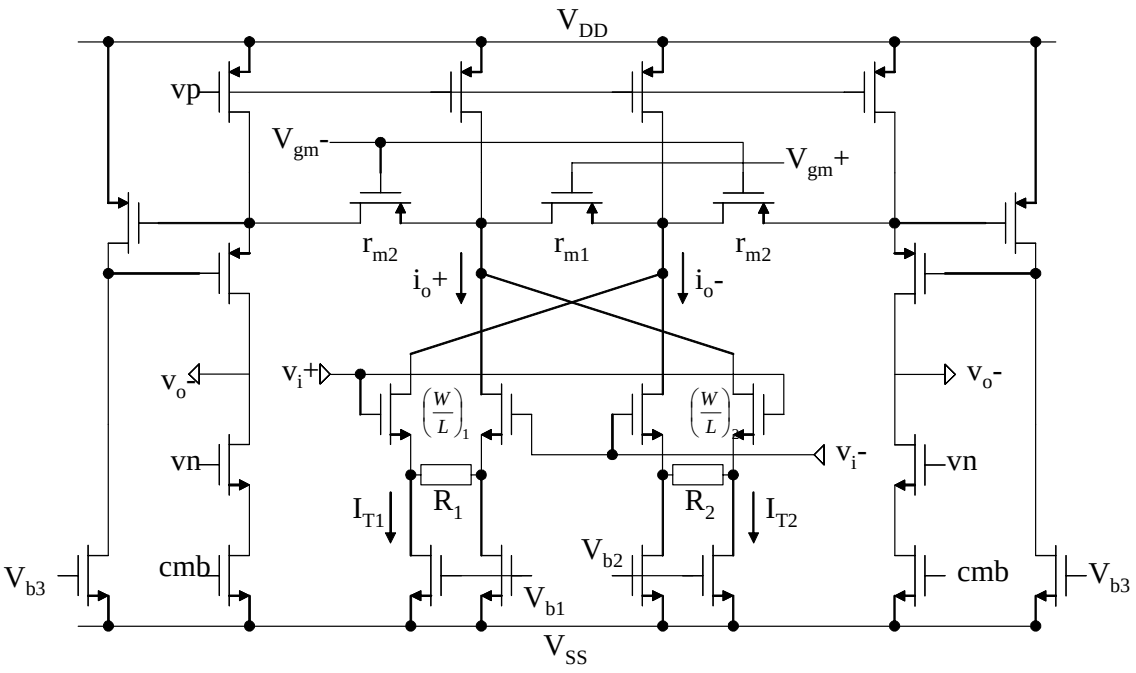


Fig. 2.12 OTA design.

A transconductance control is incorporated in order to provide frequency tuning for the filter. For that matter, the variation of I_{T1} and I_{T2} is not a good option because it modifies V_{dsat1} and V_{dsat2} changing the linearity properties and also it affects the optimal linearity cancellation point. To provide independent transconductance control while maintaining a constant linearity, a current division approach is used as described in [26],[29]. Tail currents I_{T1} and I_{T2} are fixed and optimized for best linearity, and the transconductance is varied with the aid of triode operating transistors M3 and M4. The output current of the DDP is attenuated by a factor α which is given by:

$$\alpha = \frac{r_{m3}}{r_{m3} + 2r_{m4}} \qquad (2.53)$$

where r_{m3} and r_{m4} are the resistance values of the triode region operating transistors M3 and M4, respectively. These resistances are given by:

$$r_{m3} = \left(2K_{m3}(V_{gs3} - V_T)\right)^{-1} \qquad (2.54)$$

$$r_{m4} = \left(2K_{m4}(V_{gs4} - V_T)\right)^{-1} \qquad (2.55)$$

Since the gate voltages of M3 and M4 are controlled by V_{gm+} and V_{gm-}, α is a function of V_{gm+} - V_{gm-}. Equation (2.53) holds provided that the voltage at the source of M6 remains almost constant for any current changes thus it is desired to have a large g_{m6}. To accomplish this an inverter formed with transistors M9 and M10 provide a negative voltage gain from the source to the gate of M6 boosting its transconductance to A*gm6; A is the gain of the inverter composed by transistors M9 and M10 which in this case is around 30dB. Transistors M5-M8 form a regulated cascode output stage to enhance the output resistance.

The dimensions of the transistors were chosen using the following considerations: M1 and M2 were dimensioned to achieve 280mV and 330mV with bias currents of 250μA and 330μA which results in the optimal linearity condition. Transistors M3 and M4 are designed using (2.54) and (2.55) to obtain resistances in the order of 500 ohms for optimal noise performance. The current through the transistors cascode transistors M6,M7 and M8 uses the same bias current as It1 and It2 for minimum power consumption yet enough to supply current at maximum output swings. M11 supply 1mA of current and are designed to keep a Vdsat of less than 500mV to

allow the swing at nodes x and y. Table 2.2 shows the final transistor dimensions of the OTA.

Table 2.2. Transistor sizes for the OTA. Length for all transistors is 1μm.

Transistor	Width (μm)	Id (μA)
M1	20	250
M2	40	330
M3	20	0
M4	40	0
M5	80	230
M6	160	455
M7, M8	40	450
M9	60	200
M10	80	200
M11	80	1000

The noise at the output of the OTA is a combination of the noise of the OTA core (transistors M1 and M2), the resistor divider (M3 and M4) and the cascode transistors. The approximate output thermal noise density of the OTA is given by:

$$\frac{I_o^{\,2}}{Hz} = 8\gamma kT\left[g_{m8} + g_{m5} + g_{m11}\alpha^2 + 4\frac{g_{m9}+g_{m10}}{(g_{m10}r_a)^2} + \frac{2}{\gamma \cdot r_a} + \alpha^2\left(\frac{(N_{r1}/(2\gamma)+1)g_{m1} + N_{r1}^{\,2} g_{mT1}}{(1+N_{r1})^2} + \frac{(N_{r2}/(2\gamma)+1)g_{m2} + N_{r2}^{\,2} g_{mT2}}{(1+N_{r2})^2} \right) \right] \quad (2.56)$$

where $r_\alpha = r_{m3} + 2r_{m4}$. There are several observations in this expressions: the larger r_α the lower the noise but a large increase in these resistances brings the parasitic pole $w_p = 1/(\alpha r_{m4} C_p)$ to lower frequencies limiting OTA's frequency response; C_p is the overall parasitic capacitance at the nodes x and y. The noise of transistors M9 and M10 is attenuated by the gain $A = g_{m10} r_a$ which is around 30, therefore its noise contribution is not important.

2.3.2 Filter design

Wire line applications, such as VDSL, contemplate next generation bandwidths up to 20MHz. To test the double differential pair concept, a 20MHz second order low-pass filter is designed. The filter is based on a ladder prototype presented in fig. 2.13.

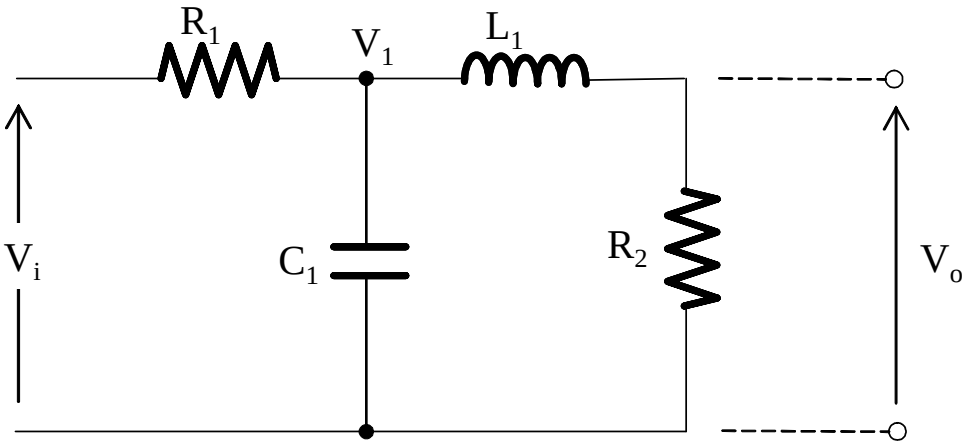


Fig. 2.13. Second order ladder low-pass prototype.

The filter is simulated using five identical OTAs as shown in Figure 2.14. The OTA transconductance can be adjusted between 70 to 160μA/V; The capacitor values are 400 fF each. An output buffer based on the same OTA is used to measure the output voltage. Due of the differential nature of the OTAs, common mode feedback (CMF) blocks are used to keep the output stages balanced around the reference voltage.

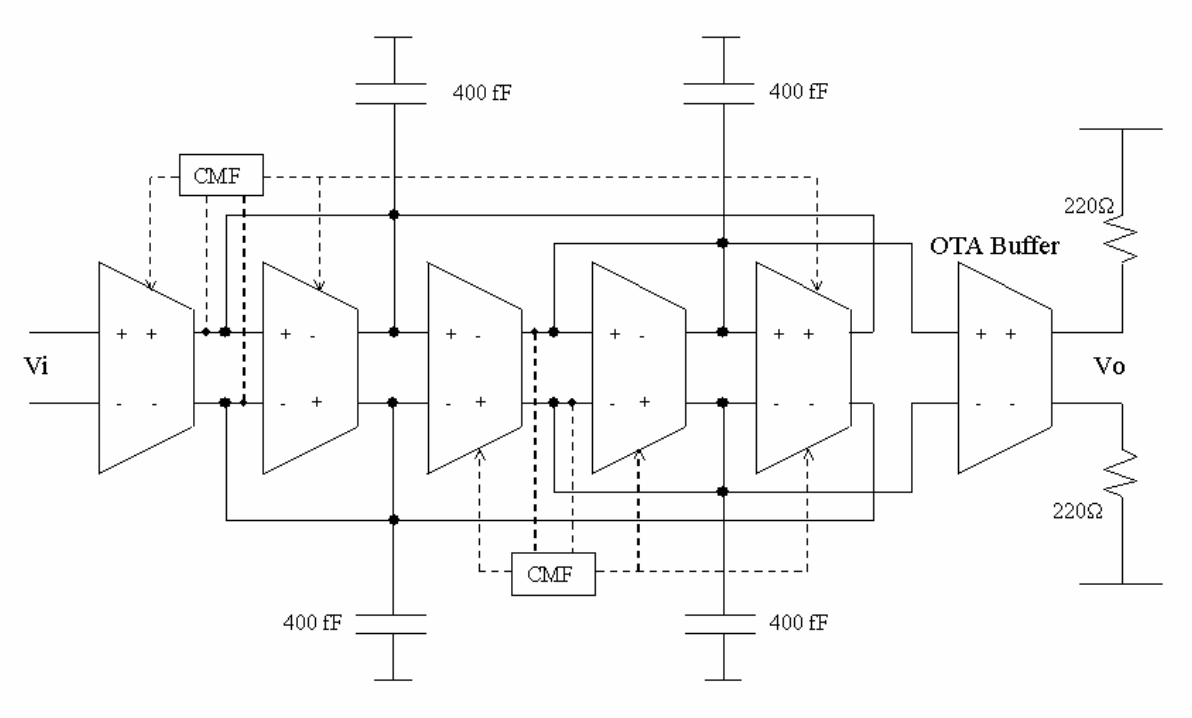


Fig. 2.14. Low-pass OTA implementation of the ladder filter.

The relation between $(R_1+R_{\theta 1})$ and $(R_2+R_{\theta 2})$ in (3.32) can varies from die to die (process variations) because of tolerances in both sheet resistance (used to implement the polysilicon resistance) and mobility degradation factor. An extra test OTA (TOTA) is used to provide information about the linearity as illustrated in fig. 2.15. Based on this, a

fine bias external adjustment is possible; since all OTA's used in the filter are the same, the adjustment of the bias condition for maximum linearity in the TOTA optimizes the linearity of the overall filter as well. For testing purposes, the linearity observation of the TOTA is done by applying two tones at the input and measure the IM3 using a spectrum analyzer at the output. For future versions, on-chip precision circuits (such as switched capacitor) are contemplated to implement the linearity adjustment in automatically.

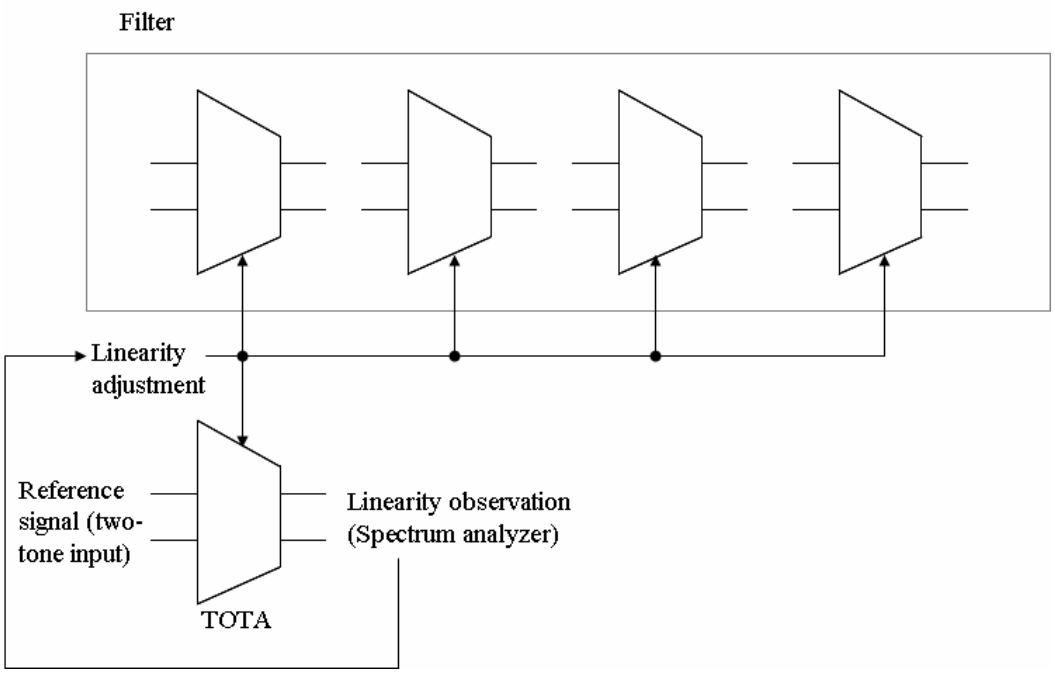


Fig. 2.15. Linearity adjustment using a test OTA (TOTA).

2.3.3 Experimental results

Figure 2.16 shows the micrograph of the chip where the active area is 0.45mm^2. The chip was fabricated in a standard CMOS 0.35μm process through the MOSIS educational service. In the test set-up, waveform generators are used to provide the input

signals and a balun is used to convert them from single-ended to differential. At the output, 50 ohm resistances are used as load for the OTA buffer and another balun is used to convert the differential output signal into single-ended; the signal is then analyzed using a spectrum analyzer.

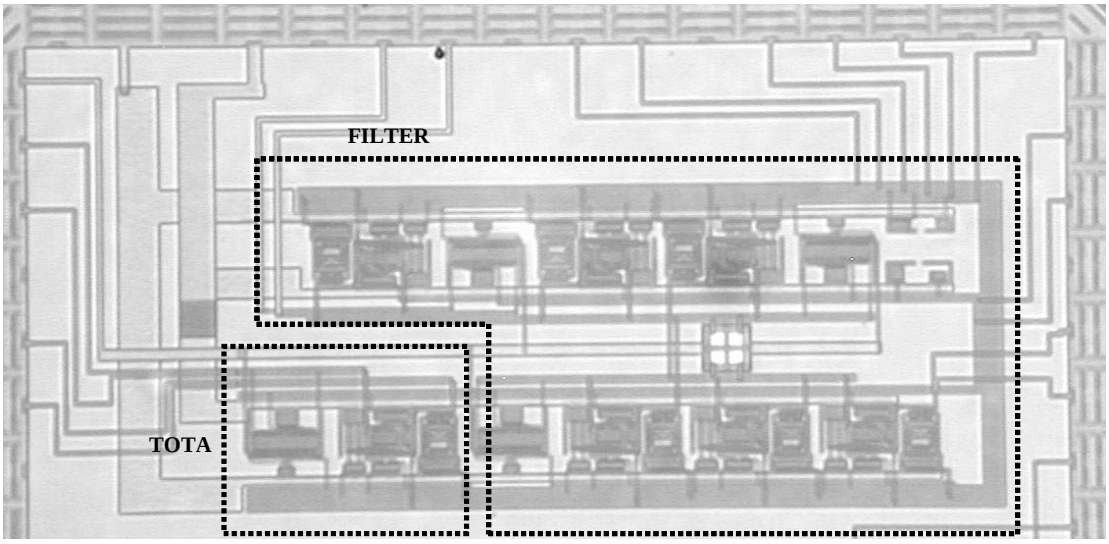


Fig. 2.16. Micrograph of the chip.

Two sinusoidal tones separated by 100kHz around 20MHz with a total amplitude of 1.3 Vpp were used to test the circuits. Figure 2.17 shows the IM3 of the TOTA and the entire filter as function of the current I_{T2}; I_{T1} has been fixed at 150 μA and 200 μA, respectively. The tail current at which optimal IM3 is achieved for the TOTA optimizes the linearity of the entire filter as well.

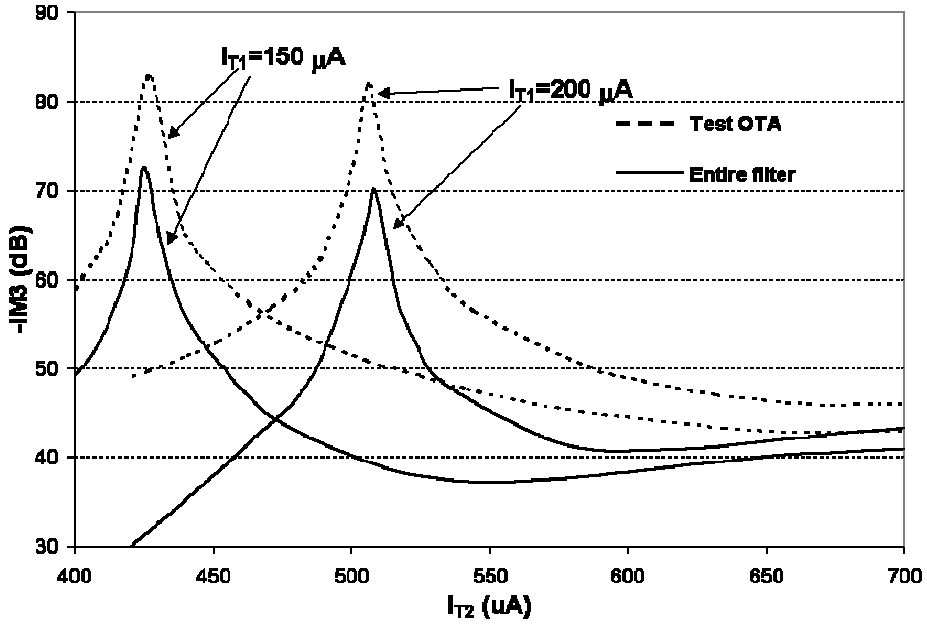


Fig. 2.17. IM3 of the filter and TOTA for several currents IT1 and IT2.

The IM3 measurement of the TOTA is below -70dB for the whole range of frequencies up to 50 MHz. Figure 2.18 shows the effect of the transconductance control on IM3. The transconductance can be controlled from 70 µA/V to 160 µA/V and IM3 is better than -70 dB. This corroborates that the transconductance control is indeed almost independent of linearity.

Figure 2.19 shows the IM3 measurement at 20MHz for the filter at 1.3Vpp input. Here, IM3 remains below -65dB over the entire filter's pass-band. The transconductance control allows to change the cut-off frequency from 12 to 24 MHz as shown in figure 2.20. The noise floor that can be appreciated at high frequencies is caused by parasitic capacitances present in the circuit board. Table 2.3 summarizes experimental results of the TOTA and the filter.

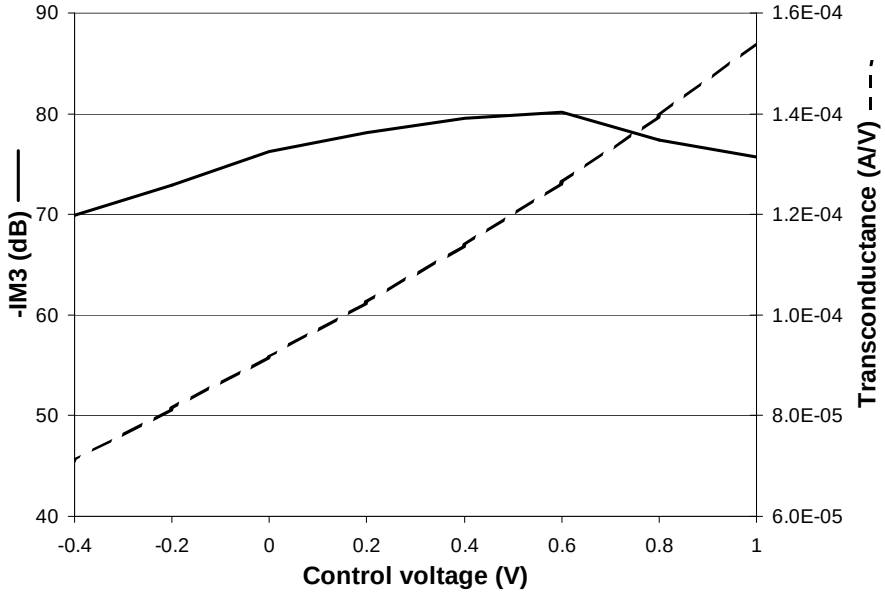


Fig. 2.18. Effect of the transconductance control over the IM3.

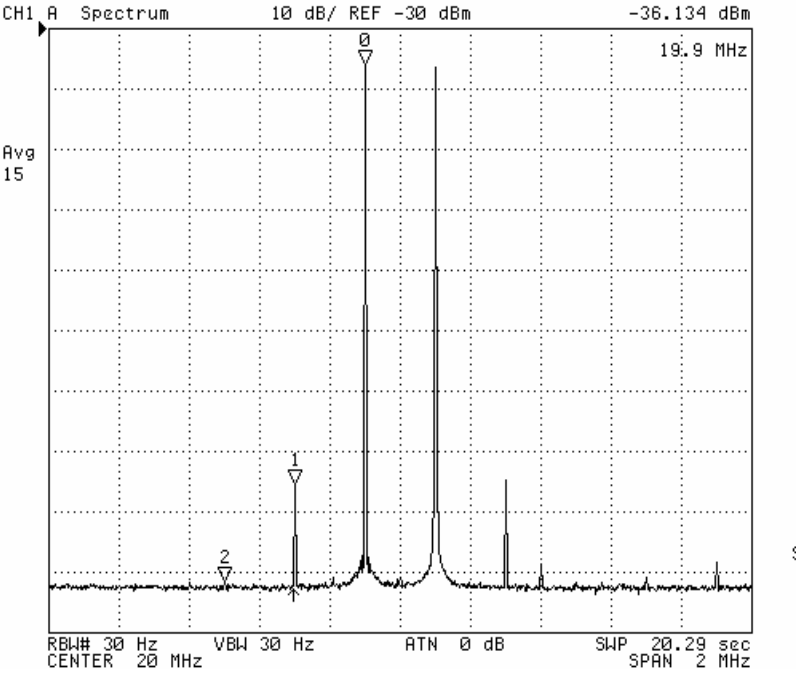


Fig. 2.19. IM3 measurement at 20Mhz, 1.3 Vpp input.

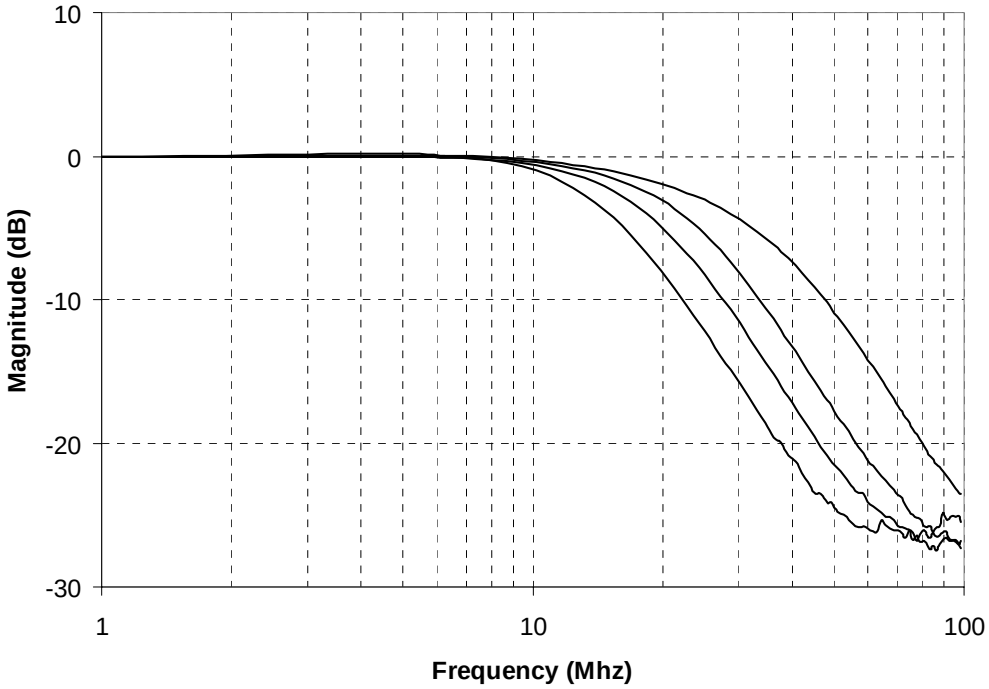


Fig. 2.20. Programmable frequency responses of the filter.

Table 2.3. Summary of experimental results of the filter.

Technology.	CMOS 0.35 μm
Supply voltage.	3.3 V
OTA	
Power consumption per OTA.	10.5 mW
Transconductance range.	70 – 160 μA/V
OTA IM3 up to 50MHz @1.3Vpp input.	<-70dB
Input referred noise	75 nV/√Hz
SNR @ 20 MHz	62 dB
Filter	
Filter's IM3 at 20MHz	
PSRR+, PSRR-	>50 dB
Input referred noise	6 μV/√Hz
SNR of the filter. (20 Mhz bandwidth)	55 dB

For the purpose of comparing the filter performance with reported schemes, the same figure of merit as defined in (1.2) will be used. Figure 2.21 shows where the described filter stands in reference to others. The proposed scheme, however, has several features that other filters do not:

- Due to the transconductance control incorporated with transistors M3 and M4, there is a nominal loss of half the transconductance because part of the output differential current flows intro transistor M3 rather. However, this feature allows a large continuous tuning range of about ±30% with minimal linearity degradation.
- Thanks to the regulated cascode output stage, the output resistance is considerably large; therefore this OTA can be used for high-Q applications. The drawback, is that the regulated cascode stage consumes 6mW which is 60% of the overall OTA power. Without the regulated cascode stage, the filter would consume half the power at the expense of lower output impedance.

Although the OTA require power consumption and has increased noise to incorporate the above mentioned features, it is still on the trend line in filters thanks to the proposed linearity techniques using the DDP.

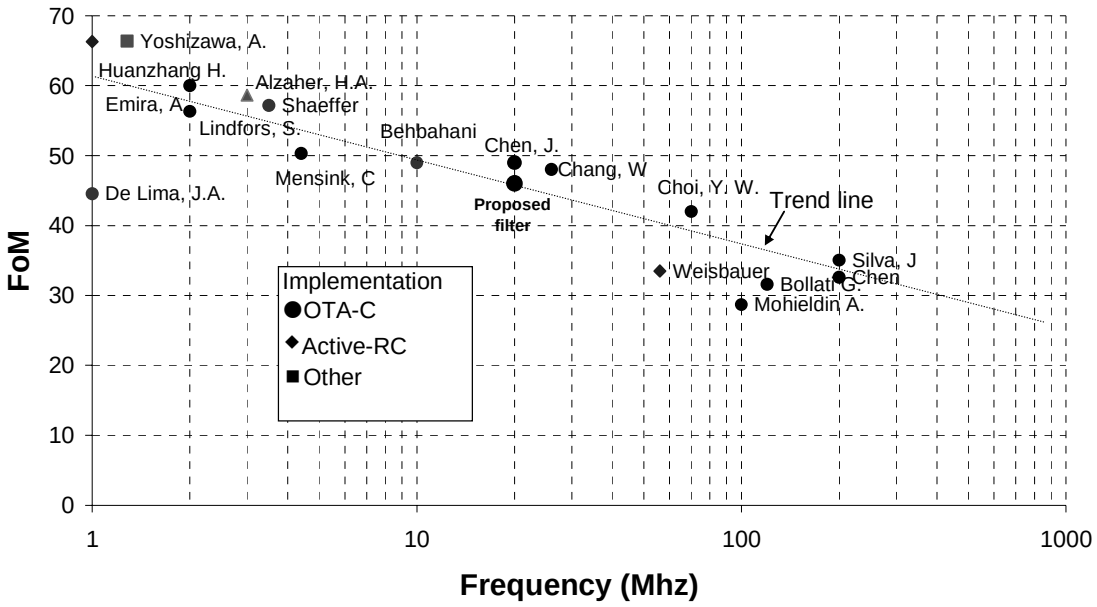


Fig. 2.21. Figure of merit of the filter in comparison with the state of the art in filters.

2.4 The triple differential pair

2.4.1 Analysis

It has been shown that the double differential can be used to reduce OTA non-linearities but the optimal cancellation is very sensitive to process variations and requires external adjustment. This is due to the fact that the cancellation relies on matching physical parameters such as V_{dsat}, R_θ and G_m that cannot be accurately controlled or predicted.

The alternative is to use equal DPs with same linear properties but different input voltages. This can be done exploiting the differential nature of the DPs; if one of the inputs of the DP is grounded, the output will be the function of half of the input voltage.

Figure 2.22 shows the block diagram of one degenerated differential pair split in three. The three DPs use the same saturation voltage and equal degeneration factors but different transistor aspect ratios. Two of the DP's (most left and most right) have one of the input terminals connected to ground and, due to the differential nature of DPs, their output current is a function of both differential and common-mode input signal. The overall circuit, however, behaves as a true differential circuit because any common mode input produces differential output current in the DPs with one terminal grounded, but due to the cross-coupled connection they cancel each other. The third DP located at the middle, is connected to both inputs as a conventional DP with tail current and uses the full input signal.

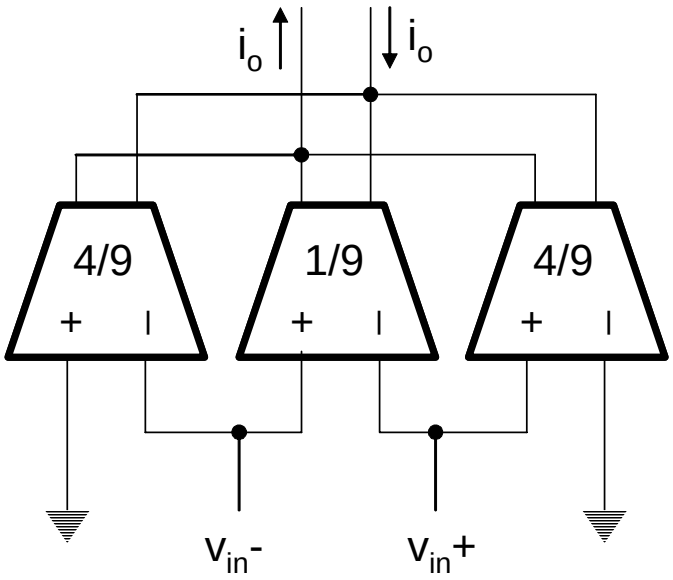


Fig. 2.22. The triple differential pair block diagram.

For the analysis of the topology, it is considered that the input signals are composed by differential and common-mode signal components such as $v_{in+}= v_{in}/2 + v_{cm}$

and $v_{in-} = -v_{in}/2 + v_{cm}$ (where v_{cm} is the common mode input voltage). Using (2.34) the AC single-ended output current of the circuit III is computed as:

$$\begin{aligned} i_o = & \frac{G_{m1}}{(1+G_{m1}R)}\left(\frac{4}{9}\left(\frac{v_{in}}{2}+v_{cm}\right)-\frac{4}{9}\left(-\frac{v_{in}}{2}+v_{cm}\right)-\frac{1}{9}v_{in}\right) \\ & -\frac{G_{m3}}{(1+G_{m1}R)^4}\left(\frac{4}{9}\left(\frac{v_{in}}{2}+v_{cm}\right)^3-\frac{4}{9}\left(-\frac{v_{in}}{2}+v_{cm}\right)^3-\frac{1}{9}{v_{in}}^3\right) \\ & -\frac{G_{m5}+R(G_{M1}G_{M5}-3{G_{M3}}^2)}{(1+G_{m1}R)^7}\left(\frac{4}{9}\left(\frac{v_{in}}{2}+v_{cm}\right)^5-\frac{4}{9}\left(-\frac{v_{in}}{2}+v_{cm}\right)^5-\frac{1}{9}{v_{in}}^5\right) \end{aligned} \tag{2.57}$$

yielding:

$$\begin{aligned} i_o = & \frac{1}{3}\frac{G_{m1}}{(1+G_{m1}R)}v_{in}-\frac{4}{3}\frac{G_{m3}}{(1+G_{m1}R)^4}v_{in}{v_{cm}}^2 \\ & -\frac{1}{3}\frac{G_{m5}+R(G_{M1}G_{M5}-3{G_{M3}}^2)}{(1+G_{m1}R)^7}\left(\frac{20}{3}v_{in}{v_{cm}}^4+\frac{10}{3}{v_{in}}^3{v_{cm}}^2-\frac{1}{4}{v_{in}}^5\right) \end{aligned} \tag{2.58}$$

Since v_{cm} is considerably smaller than v_{in}, (2.58) can be approximated as:

$$i_o \approx \frac{1}{3}\frac{G_{m1}}{(1+G_{m1}R)}v_{in}+\frac{1}{12}\frac{G_{m5}+R(G_{M1}G_{M5}-3{G_{M3}}^2)}{(1+G_{m1}R)^7}{v_{in}}^5 \tag{2.59}$$

Notice that the third order component is effectively cancelled regardless of physical parameters provided that v_{cm} is very small. Therefore, the non-linearities are caused mainly by the fifth order component where the THD is given by:

$$THD = \frac{5G_{m5}}{48G_{m1}(1+G_{m1}R)^5}{v_{amp}}^4 \tag{2.60}$$

Then the THD improvement over the simple differential pair is:

$$THD_{imp} = \frac{THD_3}{THD_{1,2}} = \frac{5G_{m5}}{12G_{m1}(1+G_{m1}R)^3}{v_{amp}}^2 \tag{2.61}$$

Figure 2.23 shows the circuit implementations of the degenerated DP (Circuit I), the degenerated DP with the tail current at the middle (Circuit II) and the proposed differential triple differential pair (Circuit III). A BSIM simulation was performed on these three circuits. Transistor dimensions are W_N/L_N = 180/1, V_{dssatN} = 270mV, W_T/L_T = 720/1 and V_{dssatT} = 200mV yielding G_{m1}=4.25mA/V, G_{m3}=3.6mA/V^3 and G_{m5}=6mA/V^5. The common mode voltage is 1.65V above V_{SS} and v_{amp} = 0.35V. Figure 2.24 shows the total harmonic distortion case of circuits I, II and III. On the same graph theoretical results are overlapped, showing a good agreement with the simulated ones.

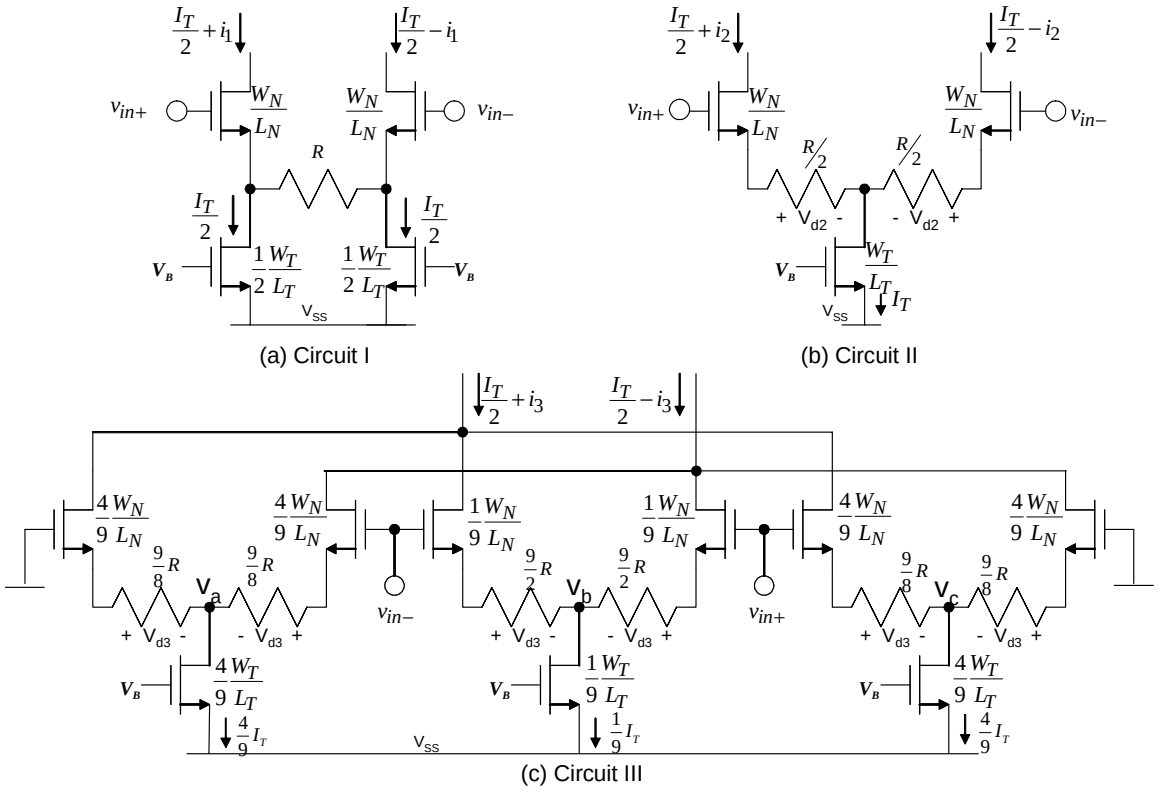


Fig. 2.23. (a) Degenerated DP, (b) degenerated DP with the tail current in the middle of the resistor and (c) proposed triple DP.

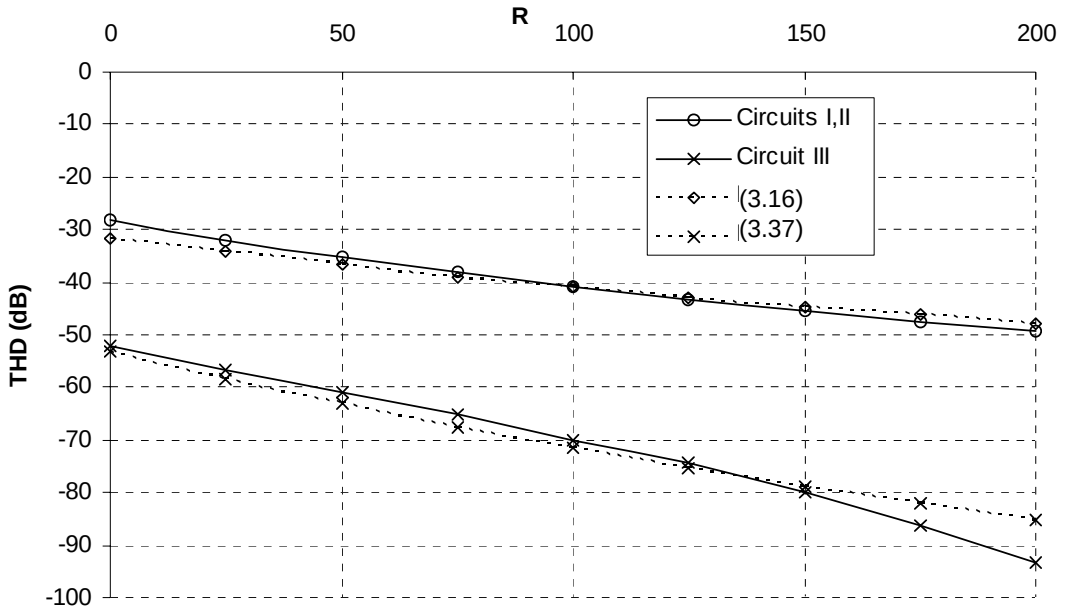


Fig. 2.24. Simulated and theoretical THD for circuits in fig. 2.23.

The advantage of this topology is that very low-distortion figures can be achieved with modest source degeneration factors that result in a small voltage drop across the resistors R; on top of that, the zero generated by R and the parasitic capacitors lumped to transistor's source is located at higher frequencies for smaller resistors. The small signal transconductance is reduced by a factor of three, as shown in (2.59), causing an increase of 9dB in the input referred noise resulting in a degradation of 9 dB in the signal to noise ratio of the topology. It will be shown that even with this drawback, better performances are achieved when compared with circuits I and II.

2.4.2 Advantages of the topology

Figure 2.25 shows Cadence simulations comparing the circuits shown in fig. 2.23. The current consumption is fixed to 3mA for all topologies. To characterize OTA's transconductance, the outputs are grounded and differential output current is measured. The parameters considered in fig. 2.25 are transconductance, third intermodulation distortion (IM3), input referred noise, and common mode transconductance. The IM3 is measured using two input tones of 0.35Vpp each one centered at 10MHz and separated by 200KHz. The common mode transconductance is defined as the ratio of the common-mode output current and the common mode input voltage. Notice that for the proposed topology, the best linearity is achieved at R=200Ω. As R is larger the DC voltage drop across it increases, limiting the signal swing at nodes v_a and v_c, the tail currents might go out of saturation region increasing the harmonic distortion components.

In order to compare the topologies, let us consider the design of an OTA with a small signal transconductance of 1 mA/V. The differential transconductance value for circuit III is obtained by using a resistor of R=100Ω; the results for this value are marked on fig. 2.25 by the vertical line A. The IM3 obtained for circuit III is around -75dB, the input referred noise density is 7.5nV/√Hz and the common mode transconductance is 60μA/V.

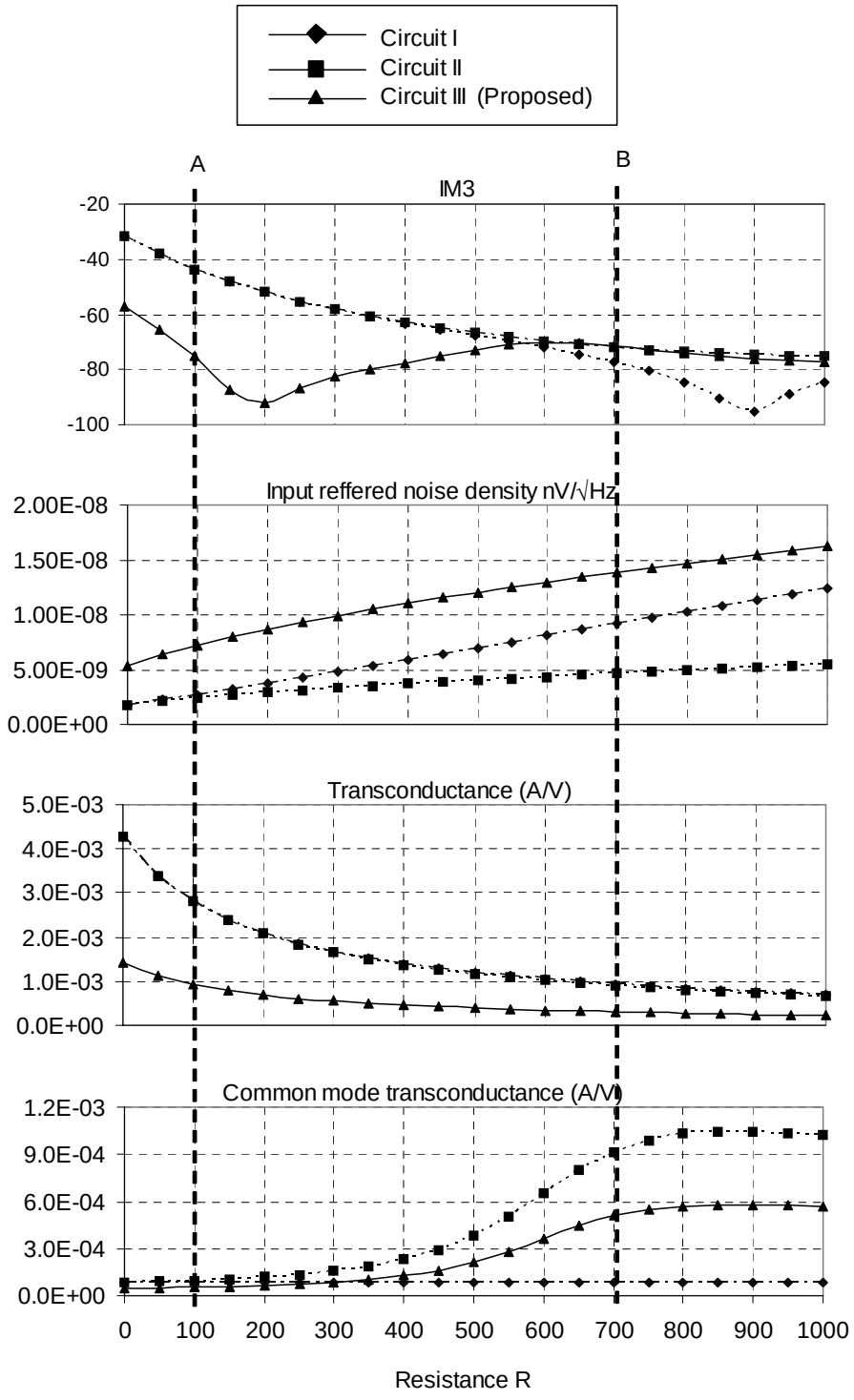


Fig. 2.25. Simulations of circuits in fig. 2.23 for different values of R.

For R=100Ω, the transconductance of circuit III is three times smaller than the one obtained for circuits I and II; as a result of the transconductance degradation, the signal to noise ratio decreases by around 9 dB. However, circuit III exhibits a superior linearity; notice that for R=100Ω (line A), an improvement in IM3 of more than 30dB is achieved; since the main limiting factor in continuous-time filters is the linearity, better balance between signal to noise ratio and signal to distortion ratio can be obtained with the proposed OTA.

Circuits I and II achieve a transconductance of 1mA/V at R=700 Ω, marked in fig. 2.25 by line B. For Circuit II, the input referred noise is still smaller than that of circuit III, but the common mode transconductance is very high. Circuit II looses part of its differential properties because the high voltage drop in R reduces the drain to source voltage of the transistor used as tail current, and may pull it into triode region.

Circuit I presents a small common mode transconductance even for high values of R. Interestingly, the linearity of circuit I at line B is comparable to that of circuit III at line A. According to (2), the IM3 should be the same for Circuits I and II but for R>600 the IM3 of the circuits is very different as a result of transistor's output resistance non-linearities caused by drain to source voltage variations; e.g. non-linear channel-length modulation. Unfortunately, these effects are not very well controlled and cannot be predicted due to the process parameter tolerances. The input referred noise level is higher for Circuit I at R=700Ω (line B) compared to circuit III at point A due to the noise contributions of the transistors used as tail current sources; hence the SNR of circuit III is better by 2 dB.

2.4.3 Complete OTA

To make Circuit III more power efficient, the proposed OTA is realized by using complementary triple differential pairs as shown in fig. 2.26. For the same amount of power, the small signal transconductance increases, improving the signal to noise ratio by another 3dB. As long as the voltage swing at each output terminal is less than half of the threshold voltage of the transistors, all transistors remain in saturation region and the output resistance is not significantly degraded. The output current is then taken directly from the drain terminals without the use of additional circuitry that contributes to additional noise and power consumption.

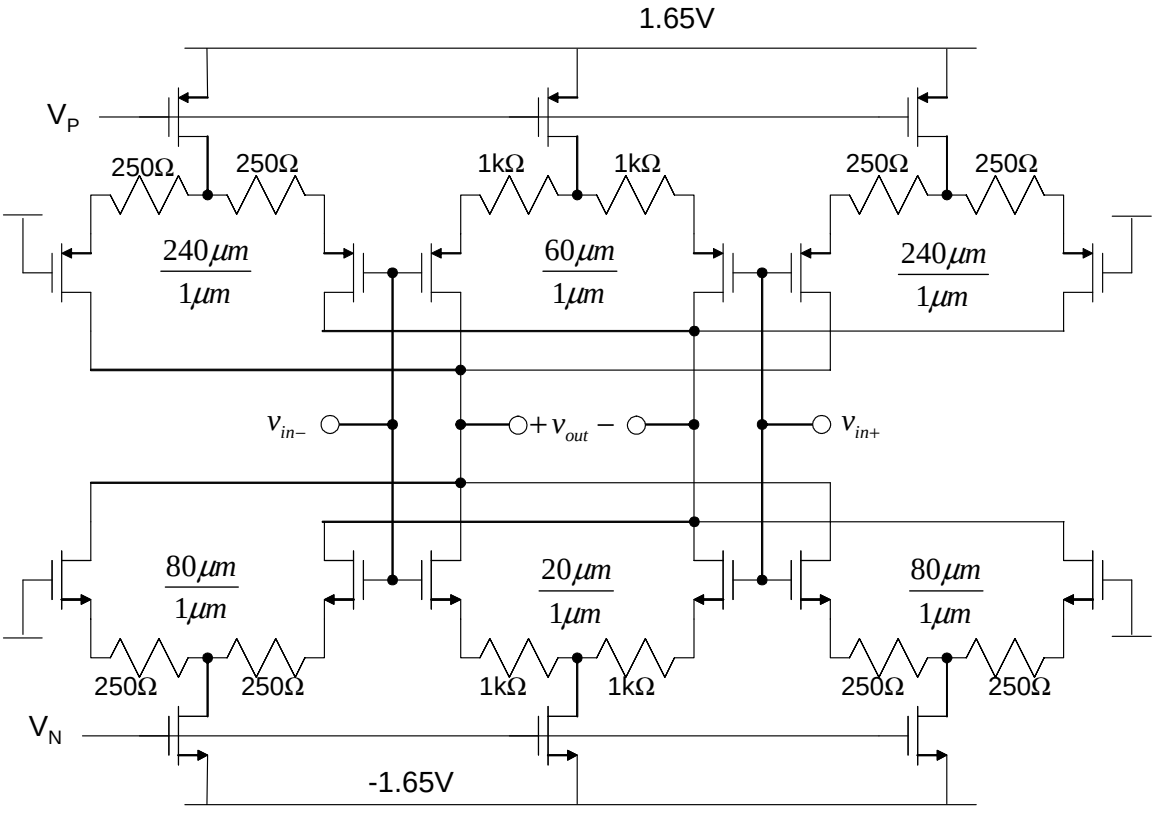


Fig. 2.26. Complete OTA using complementary triple-DP.

2.4.4 Experimental results

The OTA was fabricated in the TSMC 0.35µm CMOS process through the MOSIS educational service. Figure 2.27 shows the chip microphotograph of the proposed OTA. The active area used is 100µm x 250µm. The resistors are implemented with polysilicon layers and occupy less area than the transistors. To achieve good matching, the transistors and resistors of the three differential pairs are interdigitized. For the measurement test setup, baluns are used at the input and output to convert the single-ended signals to differential and vice versa. The OTA consumes 2.8mA of current and has a transconductance of 1.2mA/V.

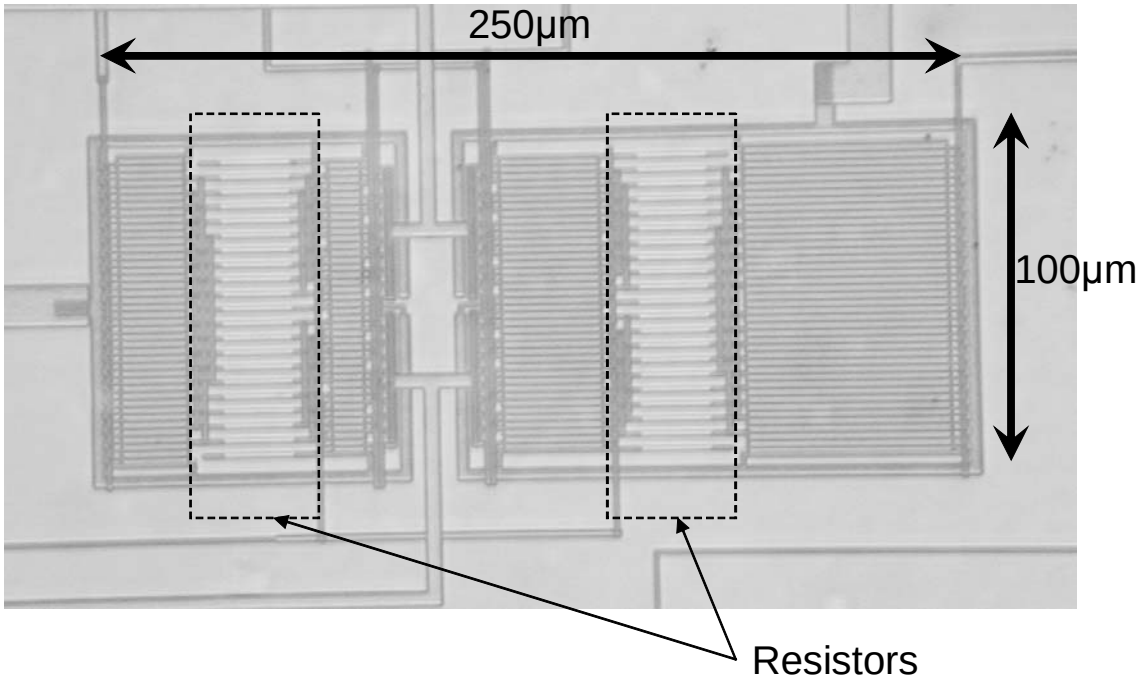


Fig. 2.27. Micrograph of the OTA.

Figure 2.28 shows the intermodulation test done for a 1.3 Vpp input signal composed by two sinusoidal inputs at 14.5 and 15.5 MHz. The measured IM3 is -77dB. Figure 2.29 presents the measurement for several frequencies ranging from 10 MHz up to 80 Mhz. The IM3 is below -70 dB for the entire frequency range. As frequency increases, the effects of the parasitic capacitances at nodes va and vb (figure 2.23(c)) are more prominent affecting the non-linearity cancellation and therefore increasing IM3.

Table 2.4 summarizes the experimental results. The OTA's input referred noise density is $7nV/Hz^{1/2}$ (theoretical minimum noise density for a transconductor of 1.2 mA/V is 4.4 $nV/Hz^{1/2}$). Even though the absence of cascode output stages, the DC gain is around 35dB due to the choice of the channel length. This gain is enough for moderate Q applications (Q<5) but may not be adequate for very selective high-Q filters. That issue may be alleviated by using negative impedance circuits [18].

Table 2.4. Summary of experimental results.

Parameter	**Value**
Technology	0.35 μm CMOS
DC Gain	35dB
Transconductance	1.2mA/V
Output resistance	50 kΩ
Input referred noise density	7nV/√Hz
IM3 @ 70MHz @ 1.3 Vpp	<-70 dB
SNR	75 dB
Power consumption	9.5 mW
PSRR± @ 70 MHz	45 dB
CMRR @ 70 MHz	40 dB
Supply voltage	3.3 V

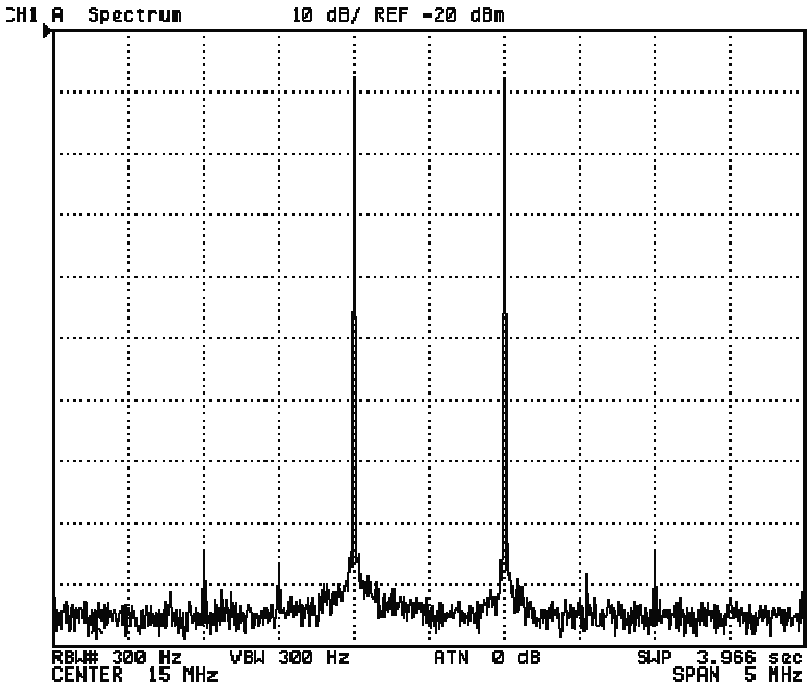


Fig. 2.28. Intermodulation test for a 1.3Vpp input at 20MHz.

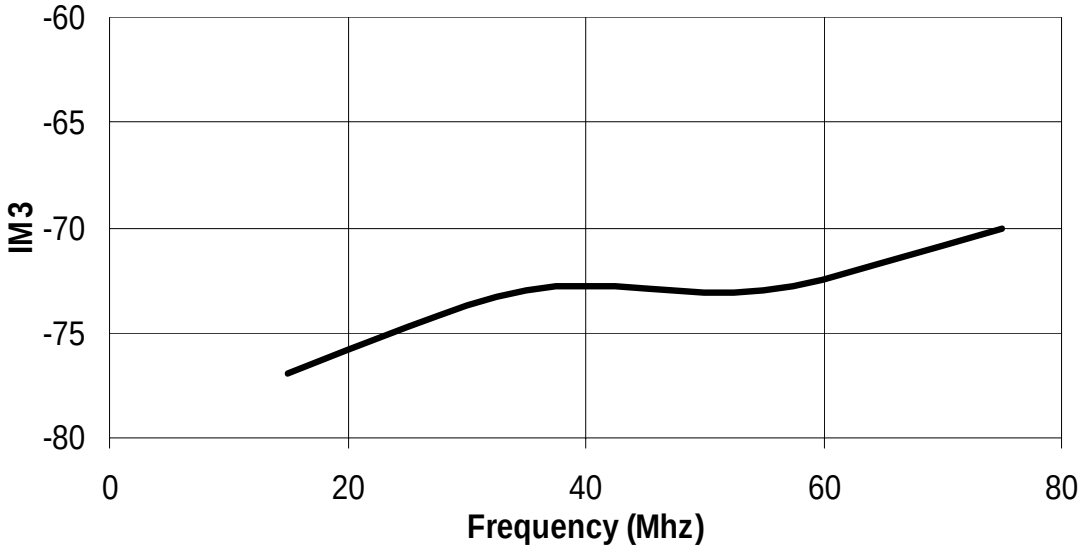


Fig. 2.29. IM3 vs. frequency.

2.4.5 Comparison with reported OTAs

Table 2.5 compares the performance of the proposed OTA with some previously reported topologies. A figure of merit (FoM) based on a normalized signal to noise ratio (NSNR) as defined in [30] and the frequency in MHz at which linearity is measured, is used:

$$FoM = NSNR + 10\log(f/1MHz) \tag{2.62}$$

In this case, the NSNR is normalized to a bandwidth of 1MHz, an IM3 of -60dB and a power consumption of 1mW.

The comparison with other topologies [31]-[36] is difficult because they may include common mode feedback circuitry and/or high impedance output stages. For fairness in the FoM, the power consumption of the proposed OTA is considered twice, accounting for the power consumption of the CMFB, not included in the prototype. Still, the FoM of the proposed OTA outperforms previous publications.

Table 2.5. Comparison with recently reported OTAs.

	[31] [1]	[32][2]	[33][3]	[34][4]	[35][5]	[36][5]	This work[6]
Power consumption	1 mW	5.7mW	2.7 mW	10.5 mW	6.6mW	4mW	9.5 mW
Distortion	THD -50dB	THD -40dB	IM3 -70 dB	IM3 -65dB	IM3 -70dB	IM3 -70dB	IM3 -70dB
Input signal	1.6 Vpp	2.5 Vpp	0.6 Vpp	1.3 Vpp	1.3 Vpp	1 Vpp	1.3 Vpp
Frequency		5 Mhz	15 MHz	20 Mhz	26 MHz	20 MHz	70 MHz
Input referred noise density	?	38 nV/√Hz	7.5 nV/√Hz	75 nV/√Hz	50 nV nV/√Hz	47 nV/√Hz	7 nV/√Hz
Trans-conductance	40µS	105 µS	660 µS	100µS	340µS	130µS	1200 µS
Supply voltage	3.3 V	5V	3.3 V	3.3V	3.3V	3.3V	3.3V
Technology	CMOS 0.35µm	CMOS 0.5µm	CMOS 0.6 µm	CMOS 0.35µm	CMOS 0.35µm	CMOS 0.35µm	CMOS 0.35 µm
FoM	-	56	97	80	85	86	103

[1] Noise was not reported.
[2] Limited linearity and small transconductance.
[3] Pseudo-differential structure.
[4] Requires manual tuning for optimal linearity; large DC gain and large tuning range stage included.
[5] Tunable and large DC gain.
[6] Does not include common mode feed-back; modest DC gain and tail current gives limited tuning range. Since the test circuit does not include CMF or a high output impedance stages, the power consumption is considered twice for the computation of FoM.

3. LINEARITY TECHNIQUES BASED ON NON-LINEAR SOURCE DEGENERATION

Techniques based on non-linearity cancellation between multiple differential pairs provide an important improvement in linearity but the drawback is that the subtraction of signals reduces the overall transconductance notably, therefore resulting OTA's power efficiency is limited and SNR is not the optimal. In this section, a technique based on non-linear degeneration is proposed where the linearity of a degenerated differential pair is improved more than 10dB with transconductance degradation of less than 10%, small extra power. Using this technique, a fifth order 30-Mhz low-pass filter is implemented achieving a spurious free dynamic range (SFDR) of 65dB with 85mW of power consumption.

3.1 Non-linear degeneration principle

The fundamental concept consists in adding to the source degeneration resistance a small non-linear element that provides the extra current needed by the differential pair to compensate its non-linear behavior. Figure 3.1 shows the degenerated differential pair with a non-linear source degeneration; depending on the voltage across the resistance, the non-linear resistor injects additional current such that the equivalent degeneration resistance reduces as the magnitude of the input signal is larger. As a result, the small signal transconductance may remain constant for a significantly larger input range. The

non-linear resistance can be accomplished with the introduction of a small cross-coupled auxiliary differential pair (ADP) without degeneration as shown in figure 3.2.

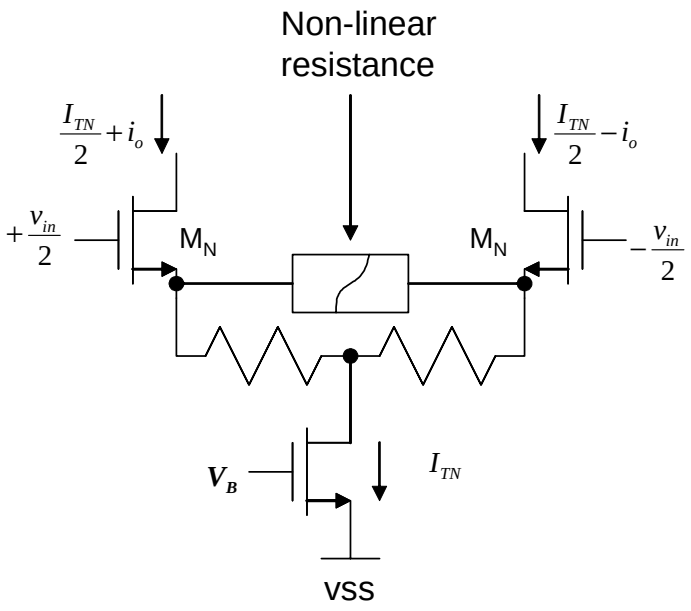


Fig. 3.1. Non-linear degeneration resistance DP concept.

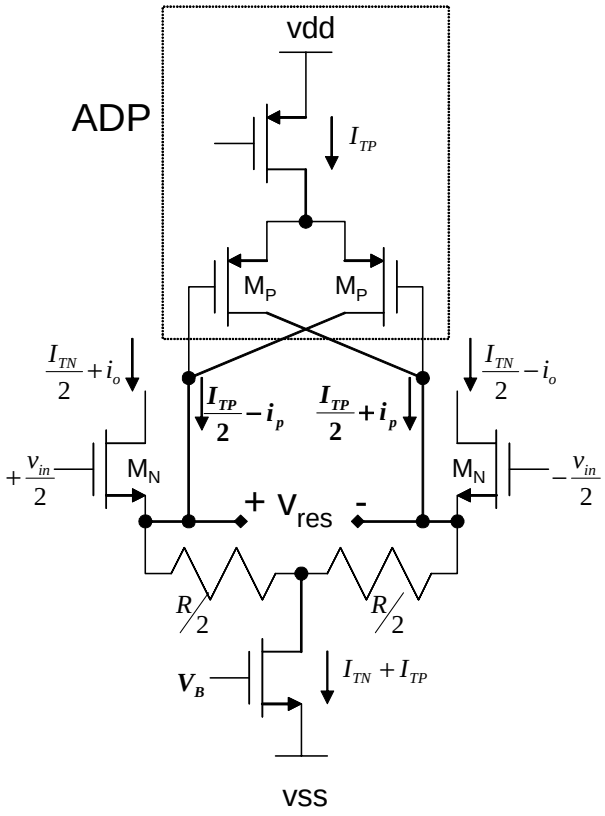


Fig. 3.2. Implementation of the non-linear resistor using an auxiliary differential pair (ADP).

To simplify the analysis of this circuit, weak non-linearities are assumed where the distortion is mainly caused by the third order term. Therefore, only the first and third order terms will be considered in the manipulation of equations.

From the analysis in section 2, the output current of the differential pair with source degeneration considering the first two terms only, is:

$$i_o = G_{M1N}(v_{in} - v_{res}) + G_{M3N}(v_{in} - v_{res})^3 \qquad (3.1)$$

where G_{M1N} and G_{M3N} are the first order and third order transconductances of the differential pair composed by transistors M_N shown in figure 3.2. Precise values of G_{M1N} G_{M3N} can be obtained using circuit's simulators with complex transistor's models such as BSIM. However, a rough approximation based on the saturation square model and taking into account the mobility degradation effect due to the lateral and fields, represented as an equivalent resistor at the source [28] lead to,

$$G_{MN1} = \frac{1}{2} \frac{\sqrt{K_N \left(W_N / L_N \right) I_T}}{1 + \frac{2}{E_{sat}} \sqrt{\frac{I_T}{W_N L_N K_N}}} \qquad (3.2)$$

and,

$$G_{MN3} = -\frac{G_{M1}}{8 \left(\frac{I_T L_N}{K_N \cdot W_N} \right) \left(1 + \frac{2}{E_{sat}} \sqrt{\frac{I_T}{W_N L_N K_N}} \right)^3} \qquad (3.3)$$

where K_N is the technological constant typically around $100\mu A/V^2$. W_N and L_N are the width and length of transistor M_N, respectively. I_T is the tail current and E_{sat} is the critical electric field with a typical value of 8.3 V/μm for the technology used.

In a typical degenerated differential pair the output differential current flows through the resistor. However, in the case of the circuit of figure 3.2, the total differential output current is the current flowing through the resistor minus the output current of the ADP i_p (the minus sign is due to the cross coupled connection), then:

$$\boldsymbol{i_o = v_{res} / R - i_p} \qquad (3.4)$$

Considering the first two terms, the current of the ADP is given by:

$$i_p = G_{M1P} v_{res} + G_{M3P} v_{res}^{\ 3} \qquad (3.5)$$

where v_{res} is the voltage across the resistance R and the ADP, G_{M1P} is the small signal transconductance and G_{M3P} the non-linear coefficient for the ADP (the minus sign is due to the cross-connection of the devices). G_{M1P} and G_{M3P} can be roughly approximated as:

$$G_{M1P} = \frac{1}{2} \frac{\sqrt{K_P \left(W_P / L_P \right) I_{TP}}}{1 + \frac{2}{E_{sat}} \sqrt{\frac{I_T}{W_P L_P K_P}}} \qquad (3.6)$$

$$G_{M3P} = -\frac{G_{M1P}}{8 \left(\frac{I_{TP} L_P}{K_P \cdot W_P} \right) \left(1 + \frac{2}{E_{sat}} \sqrt{\frac{I_{TP}}{W_P L_P K_P}} \right)^3} . \qquad (3.7)$$

Then (3.5) becomes:

$$i_o = (R^{-1} - G_{M1P}) v_{res} - G_{M3P} v_{res}^{\ 3} \qquad (3.8)$$

Combining this equation and (3.1) yields,

$$G_{M1N} (v_{in} - v_{res}) + G_{M3N} (v_{in} - v_{res})^3 = (R^{-1} - G_{M1P}) v_{res} - G_{M3P} v_{res}^{\ 3} \qquad (3.9)$$

Due to the third order nature of the above equation, the procedure to obtain the solution for v_{res} can be tedious. However, if the solution is expressed in a series expansion given by:

$$v_{res} = \sum_{n=0}^{\infty} C_{(2n+1)} v_{in}^{\ (2n+1)} \qquad (3.10)$$

where coefficients C1,C3,… are unknown, and then (3.10) is substituted into (3.9), the resulting equation arranged in a series of powers of v_{in} yields (for simplicity only the first two terms are shown):

$$0 = \left[G_{M1N} - C_1\left(G_{M1N} + R^{-1} - G_{M1P}\right)\right]v_{in} + \left[G_{M3N}(1-C_1)^3 + G_{M3P}C_1{}^3 - C_3\left(G_{M1N} + R^{-1} - G_{M1P}\right)\right]v_{in}{}^3 . \quad (3.11) + \ldots$$

Notice that for (3.11) to hold true, each of the coefficients of the terms multiplying vin^n must be zero. Then, C_1 can be solved directly from the first term regardless of the consideration of higher order terms. Then:

$$C_1 = \frac{G_{M1N}}{G_{M1N} + R^{-1} - G_{M1P}} \qquad (3.12)$$

Once C_1 is found, C_3 can be found from the second term and yields:

$$C_3 = \frac{(R^{-1} - G_{M1P})^3 G_{M3N} + G_{M3P} G_{M1N}{}^3}{(G_{M1N} + R^{-1} - G_{M1P})^4} \qquad (3.13)$$

If one is interested in C_5 and other coefficients, higher order term must be considered as well but for our weak non-linearity analysis, fifth order and higher components are assumed to have an irrelevant contribution to the result; therefore we are interested in C1 and C3 only. Then using (3.12) and (3.13) into (3.11) gives:

$$v_{res} = \frac{G_{M1N}}{G_{M1N} + R^{-1} - G_{M1P}} v_{in} + \frac{(R^{-1} - G_{M1P})^3 G_{M3N} + G_{M3P} G_{M1N}{}^3}{(G_{M1N} + R^{-1} - G_{M1P})^4} v_{in}{}^3 \qquad (3.14)$$

Finally, (3.14) can be used in (3.1) to obtain:

$$i_o = \frac{G_{M1N}}{1 + \frac{RG_{M1N}}{1 - RG_{M1P}}} v_{in} + \frac{G_{M3N} - G_{M3P}\frac{G_{M1N}{}^4}{(R^{-1} - G_{M1P})^4}}{\left(1 + \frac{RG_{M1N}}{1 - RG_{M1P}}\right)^4} v_{in}{}^3 \qquad (3.15)$$

Then, the third order term can be eliminated if the following condition occurs:

$$\frac{G_{M3N}}{G_{M3P}} = \left(\frac{G_{M1N} R}{1 - G_{M1P} R} \right)^4 \qquad (3.16)$$

The effective small signal source degeneration resistance (~ $R/(1-G_{M1P}R)$) increases due to the effect of the ADP; hence to minimize the main transconductance degradation it is desirable to design the topology such that $G_{M1P}R<<1$. Additionally, since the right hand term of (3.16) is elevated to the power of four, the ratio between G_{M3N} and G_{M3P} can be large even for modest degeneration factors ($N_r=G_{M1N}R$). Therefore, since G_{M1P} and G_{M3P} are smaller compared with G_{M1N} and $G_{M3N,}$ the ADP has a lower power and area requirement in comparison to the main differential pair.

To corroborate these results and observations, fig. 3.3(a) shows simulation plots of transconductance against the input voltage for different sizes of transistors M_P. For this simulation the following parameters are used: I_T=2mA, I_{TP}=125μA, G_{M1}=3.78mA/V, G_{M3}=-8.2mA/V^3 and R=500Ω. Figure 3.3(b) shows the G_{M1P} and G_{M3P} curves vs. the transistor size based on (3.6) and (3.7). The condition given in (3.16) is met when W_p/L_p = 31.2 (indicated as B); this case yields a flat transconductance response for an input range from -0.4V to 0.4V. Smaller transistor sizes indicated, with letter A, result in an under-compensated transconductance while a larger size (C) results in an over-compensated topology.

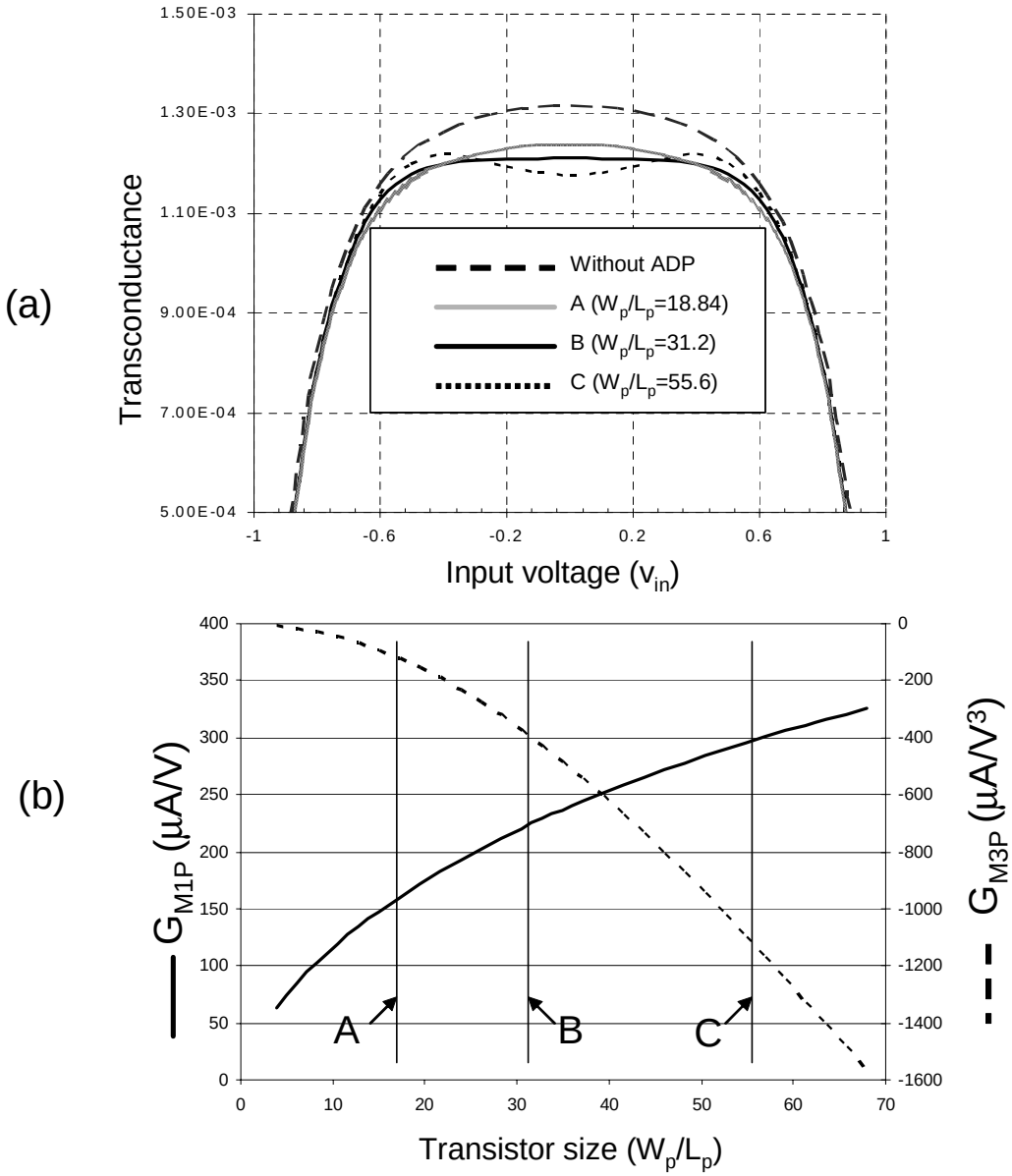


Fig. 3.3. (a) Transconductance plots for different sizes of M_P. (b) Values of G_{M1P} and G_{M3P} for different transistor sizes.

To further confirm (3.16), fig. 3.4 shows the IM3 simulated and theoretical plot vs. W_p/L_p. The theoretical IM3 of the differential pair with ADP based on (3.15) is:

$$IM3 = \frac{3}{16}\frac{G_{M3N} - G_{M3P}\dfrac{G_{M1N}{}^4}{(R^{-1} - G_{M1P})^4}}{G_{M1N}\left(1 + \dfrac{RG_{M1N}}{1 - RG_{M1P}}\right)^3} V_A{}^2 \quad (3.17)$$

where V_A is the peak voltage of the input signal (in this simulation V_A=700mV_{pp}) and G_M parameters are extracted from (3.2),(3.3),(3.6) and (3.7) . Also plotted in fig. 3.4 is the simulated IM3 without the ADP which is -53dB. The simulated IM3 is very close to the theoretical one with an error of approximately 15% in the optimal linearity point. The error is due to the use of approximate models to calculate G_{M1} and G_{M3} and the ignorance of fifth order components.

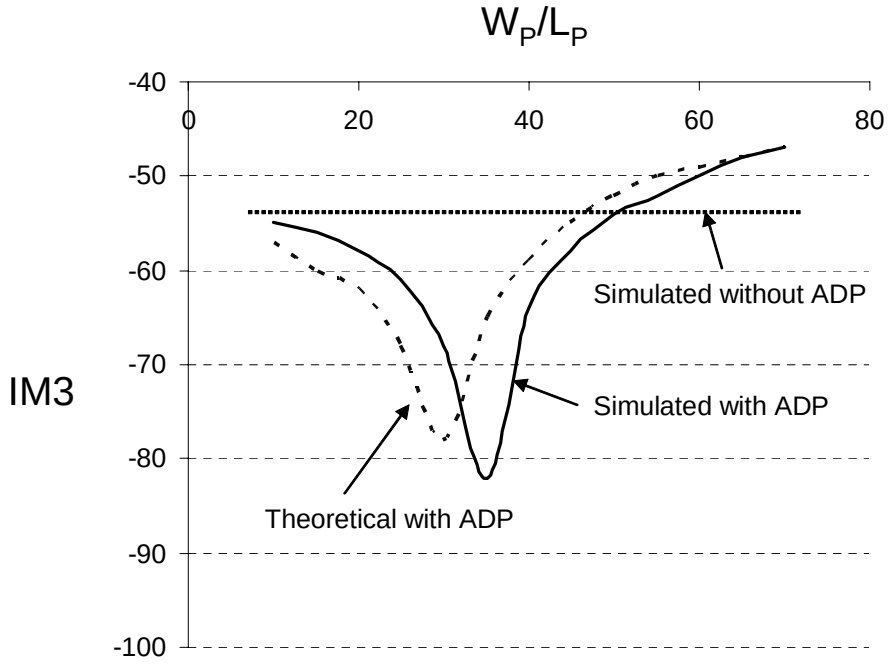


Fig. 3.4. Theoretical and practical IM3 for different W_p/L_p ratio.

For a 0.7Vpp input, the differential pair without ADP shows a third order intermodulation distortion (IM3) of -53dB with $N_r=G_{M1N}R=1.9$. With the ADP activated, only 125μA extra current is used which represents only one sixteenth of additional power ($I_{TN}=16I_{TP}$), the IM3 is reduced down to -67dB for frequencies up to 60MHz. The size of the ADP requires only 16% additional area and the overall small-signal transconductance decreases by less than 10%. Therefore an improvement over 10dB in linearity can be achieved with a negligible amount of extra power, small transconductance loss and a non-critical area increase.

An important issue is to ensure that the non-linearity suppression is effective under process parameter variations. The right hand term of (3.16) is especially critical, as it is elevated to the power of four. In this term, $G_{M1P}R$ is smaller than one and its variations are not significant but any variations in R and G_{M1N} can introduce large errors. Figure 4.5 presents the linearity improvement vs. variations of R; linearity improvement is defined as the difference between the IM3 of the differential pair with the ADP and the one without. As it can be seen, a 20% variation in R has a high impact on the linearity improvement if I_{TN} is fixed (dashed curve).

To minimize the loss of linearity improvement with the above mentioned process variations, I_{TN} can be modified to match G_{M1N} to R. If the tail current I_{TN} is controlled to adjust G_{M1N} and maintain the product of $G_{M1N}R$ constant, the IM3 improvement remains larger than 10dB for ±20% variations of R as shown in fig. 3.5 with the bold curve. Given the fact that G_{M1N} and R are first order parameters that are easily observable, a self bias circuit may be implemented based on a simple DC loop that ensures $n=G_{M1N}R$,

where n is a constant. The details of the design of the self-bias circuit are discussed in the next section.

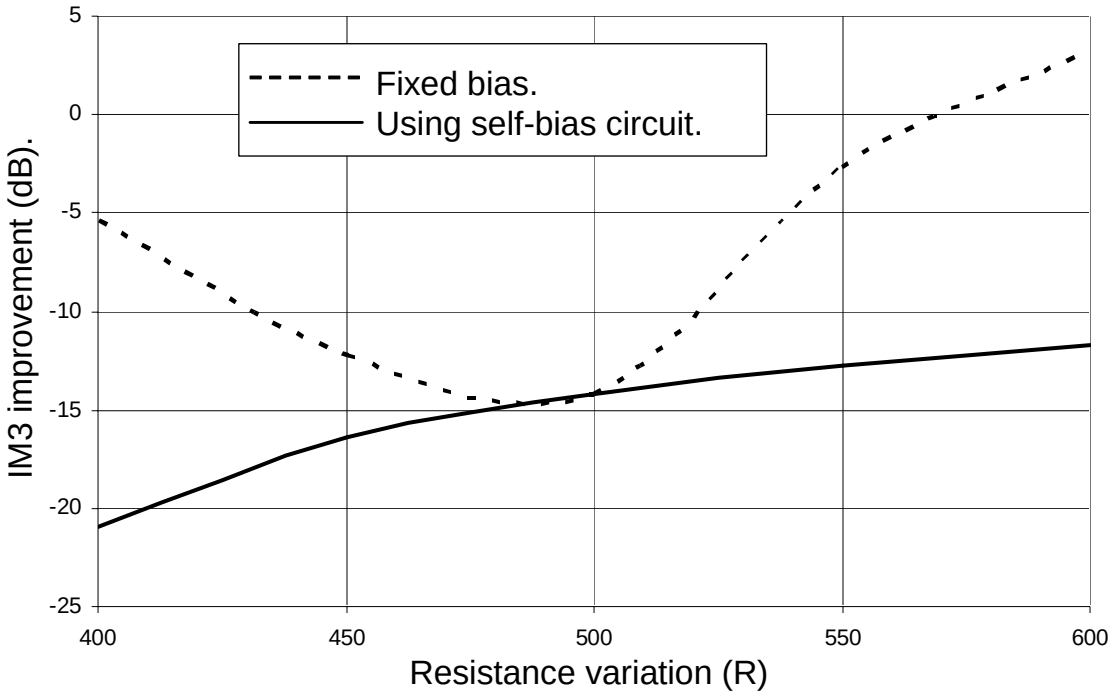


Fig. 3.5. IM3 improvement variations with and without the self-bias circuit.

Since G_{M3N} and G_{M3P} are not first order terms and correspond to different types of transistors, a matching between these cannot be assured. However, as it can be gathered from (3.16), these variations have a lower impact than R and G_{M1N}. Theoretically, a 20% mismatch between G_{M3N} and G_{M3P} will still produce a 10dB linearity improvement over a conventional degenerated differential pair. Since G_{M3N} and G_{M3P} depend on several parameters as indicated in (3.2) and (3.3), Monte Carlo simulations were carried out using random process variations around the corners for three values of R ($G_{M1N}R=n$ is enforced). Figure 3.6 shows a scatter plot relating the

third intermodulation component of the differential pair with ADP ($IM3_{adp}$) activated against the linearity of the differential pair without ADP ($IM3_n$). The traced line $IM3_{adp}=IM3_n+10$ is added for completeness.

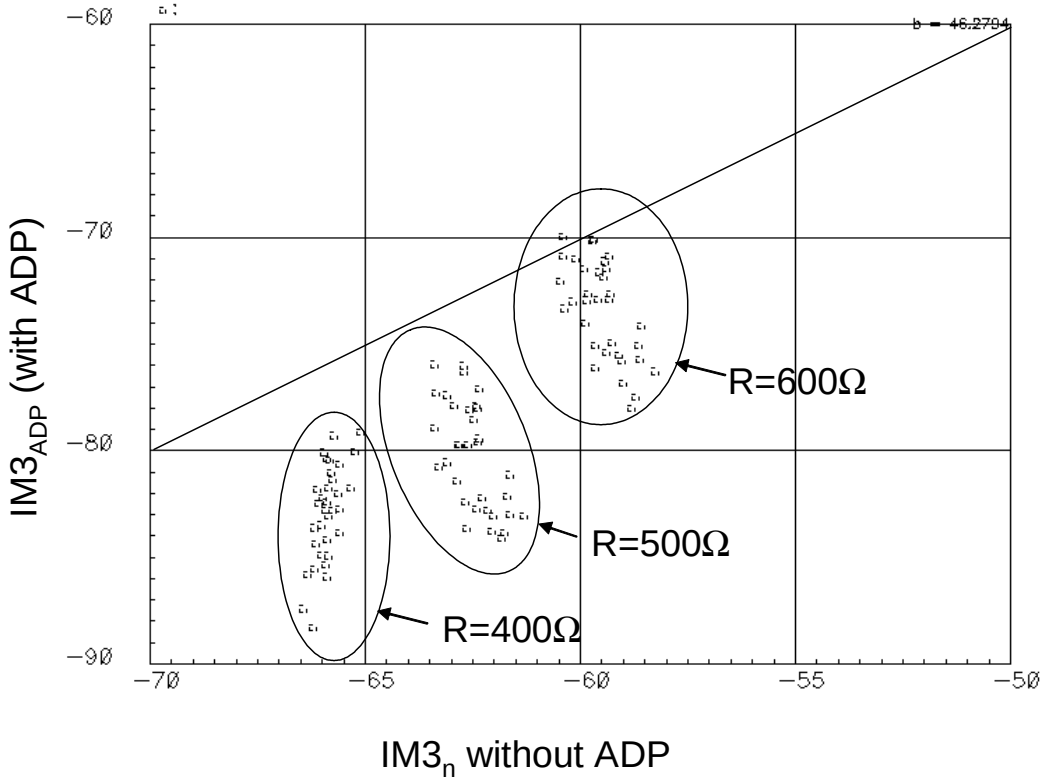


Fig. 3.6. Scatter plot of Monte Carlo simulation of IM3 with and without ADP including process parameter variations. It is shown that at least 10dB improvement in IM3 can be guaranteed.

For all cases a linearity improvement of at least 10dB can be guaranteed with the proposed linearity technique over process variations. Main parameter's variations include oxide thickness, threshold voltage, width and length etching effects all of them with 10% deviation.

The input referred noise density for the circuit in fig. 2(b) is:

$$\frac{v_{inoise}^{\ 2}}{Hz} = \frac{4kT}{G_{M1N}}\left(\gamma + \frac{N_r}{\left(1-RG_{M1P}\right)^2} + 2\frac{G_{M1P}}{G_{M1N}}\frac{\left(1+\dfrac{N_r}{1-RG_{M1P}}\right)^2}{\left(1+\dfrac{G_{M1P}}{G_{M1N}}+\dfrac{1}{N_r}\right)^2}\right) \tag{3.18}$$

The noise introduced by the auxiliary circuitry is reflected in the last term of the previous equation. Thus, since $G_{M1P}<<G_{M1N}$ the noise introduced by the ADP is not significant. Simulation results using the previous data reveal that a differential pair without the ADP the input referred noise density is 5nV/√Hz and by inserting the ADP, the noise goes up to 5.5nV/√Hz resulting in a small decrease of less than 1dB in SNR.

3.2 A 30-MHz low-pass filter implementation

In current applications using OFDM and DFT as modulation schemes, such as ADSL and video, the linearity requirement is very stringent. For instance, in ADSL (Asymmetrical Digital Subscriber Lines) cable modem applications, the linearity has to be better than 60dB and video applications require at least 60 dB of linearity at 5 MHz. Future trends pushing towards higher data transfers will require higher frequency ranges with equal or better linearity such as next generation systems power line communications that demand speeds in the order of 200Mb/s and signal bandwidth up to 30 MHz [37]. Using the non-linearity degeneration concept developed in the previous section, a filter with cut-off frequency of 30MHz with 1dB ripple and 30dB attenuation for frequencies higher than 40MHz is designed in the following subsections. The aim of the filter is to handle IM3 as well as SNR better than 60dB.

3.2.1 Design considerations

For the topology of the filter, a ladder architecture is chosen due to its low sensitivity to component variations. Figure 3.7 shows a generic low-pass ladder filter; all the inductors are floating and resistors R are used as terminations. Capacitors may also be present in parallel with the inductors (not shown in the figure) . For an integrated implementation inductors are not available and therefore they have to be emulated using gyrators as shown in fig. 3.8(a) where the simulated inductance is given by:

$$L = \frac{C}{G_1 G_2} \qquad (3.19)$$

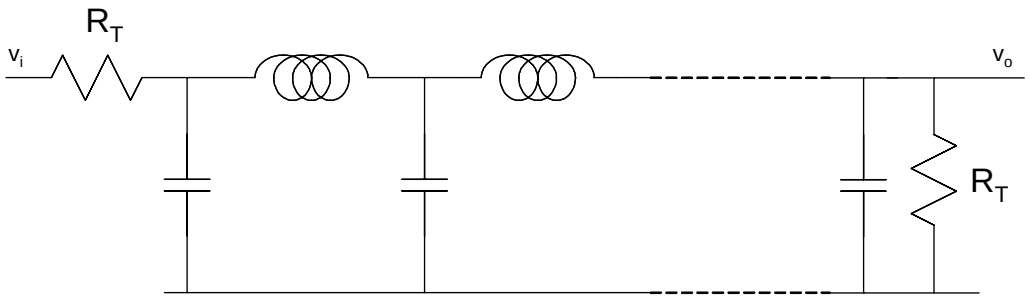


Fig. 3.7. A generic ladder low-pass filter.

Unfortunately, the transconductors used to implement the gyrator introduce noise to the system. The noise output current of the transconductor can be expressed as,

$$i_n^{\,2} = \varepsilon 4kTG \quad (3.20)$$

where ε is the noise factor of the OTA defined as the ratio of the OTA noise and the equivalent conductance noise (ε>1). The equivalent input referred noise is:

$$v_n^{\,2} = \varepsilon \frac{4kT}{G} \quad (3.21)$$

Using (3.20) and (3.21), the equivalent noise model of the circuit of fig. 3.8 (a) can be represented with an inductor with the equivalent noise sources as shown in fig. 3.8 (b).

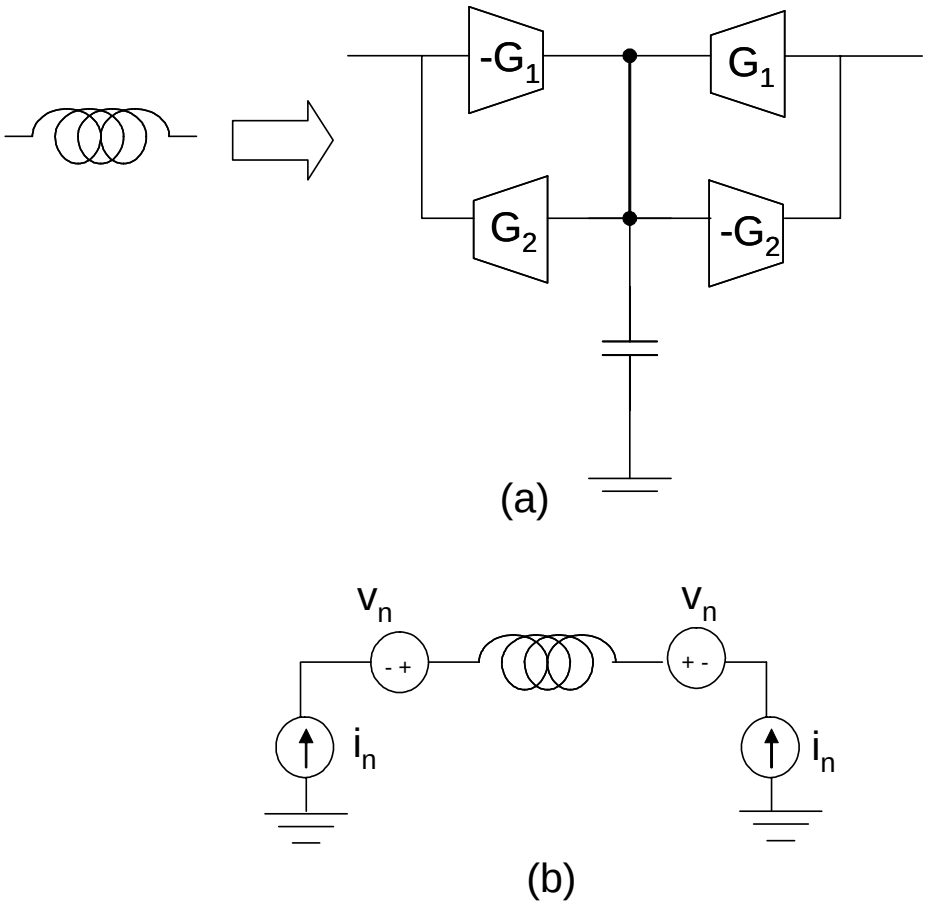


Fig. 3.8. (a) Active inductance simulation using transconductors. (b) Noise representation of the active inductor.

For the noise analysis of the ladder filter of fig. 3.7, we will consider the low frequency case for which it can be assumed that capacitors behave as open circuits and inductors as short circuits. The output noise analysis at low frequencies can be then simplified as shown in fig. 3.9 and is given by:

$$v_{on}^{\ 2} = 2\frac{4kTR}{4} + 2N_L\frac{v_n^{\ 2}}{4} + 2N_L\frac{i_n^{\ 2}R^2}{4} \qquad (3.22)$$

where N_L is the number of inductors in the filter. With (3.20) and (3.21), (3.22) yields,

$$v_{on}^{\ 2} = 2kTR\left(1 + N_L\varepsilon\left(\frac{1}{G_1R} + G_2R\right)\right) \qquad (3.23)$$

Notice from the above equation that the minimum noise can be obtained if the following condition is satisfied:

$$R = \frac{1}{\sqrt{G_1G_2}} \qquad (3.24)$$

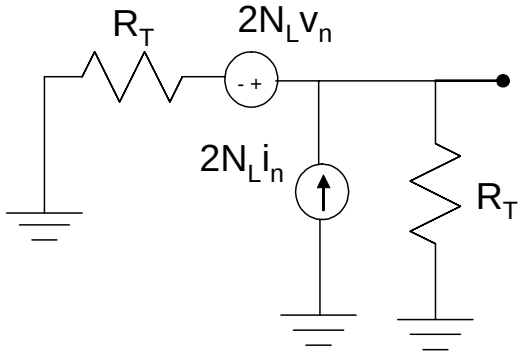


Fig. 3.9. Noise model of a ladder low-pass filter at low frequencies.

Since G1 and G2 are proportional to the current consumption, the most power efficient solution can be given for G1=G2. Then (3.23) can be approximated as:

$$v_{on}^{\ 2} \approx 4kTRN_L\varepsilon \qquad (3.25)$$

From the above equation we can gather that for noise improvement it is important to minimize the number of inductors, use an OTA with a low noise factor and maximize the transconductance.

For middle frequencies, inductors are no longer short circuits and capacitors cannot be considered open circuits anymore. In fact, the noise density of the circuit can

be higher for frequencies just below the cut-off frequency especially for filters using large Q. In the following subsection the overall noise is calculated

3.2.2 Filter structure.

In order to find out the filter structure, the required number of inductances (N_L) and capacitances for the filter, different approximations are evaluated with the aid of FilterWiz and Elsie software tools [38]-[39]. Table 3.1 shows the required order for the design of the specified filter with 30Mhz bandwidth, 1dB passband ripple and 30dB stopband attenuation at 40MHz. The elliptic approximation allows the implementation of the filter with the lower order and therefore minimum number of inductances. Furthermore, since $R=G^{-1}$ where G is proportional to the current requirement of transconductors, the use of lower N_L alleviates the power consumption.

Table 3.1 Approximation results.

Approximation	Butterworth	Chebyshev	Inverse Chebyshev	Elliptic
Order	15	7	7	5

The elliptic circuit synthesis was performed with the Elsie software. Figure 3.10 shows the elliptic ladder implementation of the filter using termination resistances of 1kΩ; the capacitances and inductances values were computed by the software according to the specifications.

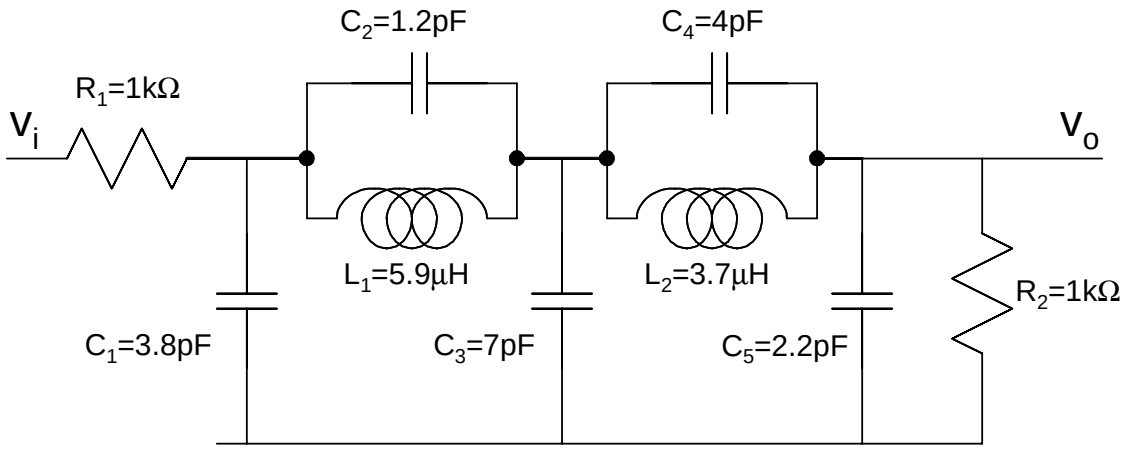


Fig. 3.10. Ladder implementation of the elliptic filter 5^{h} order.

Figure 3.11 presents the OTA-C differential implementation where eight identical OTA's are used with 1mA/V of transconductance. The total integrated output noise of this circuit is the noise contribution of each OTA multiplied by the transfer function of the output of that OTA to the filter's output. The total average noise density is then given by:

$$BW \cdot v_{n\_total}{}^{2} = \sum_{1}^{N} \int_{0}^{BW} v_{n}{}^{2} H(w)_{N}{}^{2} dw \quad (3.26)$$

Where v_n is the input referred noise of each OTA as given by (3.11) and $H(w)_N$ is the magnitude transfer function from the n-th OTA input to the output of the filter v_o. For the synthesized filter in figure 3.10 the total output noise for a BW of 40MHz using (3.26) is equal to $v_{n\_total}=1.25v_{on}$ where v_{on} is the DC noise given in (3.18). Since we attempt to have an input referred noise density of 25nV/Hz (12.5nV/Hz at the output), then:

$$\sqrt{(1.25)8kTRN_L\varepsilon} < 12.5nV/\sqrt{Hz} \qquad (3.27)$$

Then the design of the filter must satisfy the following condition:

$$RN_L\varepsilon < 4000 \quad (3.28)$$

In this implementation only two inductors are used (N_L=2); using (3.28) with termination resistances of R=1kΩ results in ε=2. The following subsections detail the design of transconductors, self bias circuit, common mode feed-back and capacitors.

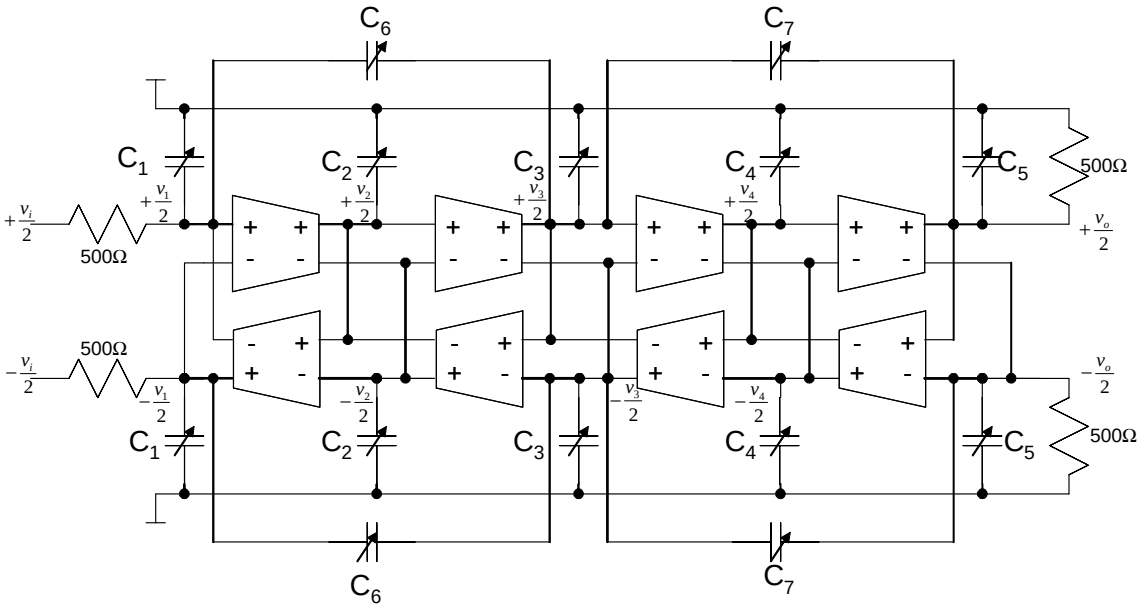


Fig. 3.11. OTA-C implementation of the filter.

3.2.3 Transconductors

Due to the ε=2 chosen, a low-noise OTA is required. Therefore, the design of the OTA consists simply in the differential pair with ADP as shown in fig. 3.12 where the output is taken directly from the drains of M_{N1} avoiding the use of folded cascoding or

any other additional circuit that contribute to more noise and power consumption. The drawback, however, is that due to the lack of cascode structures the output impedance is not very high; for very high Q filters, this problem may result in a deteriorated ripple in the filter response. Transistors M_{P3} act as current sources controlled by a V_{cmf} signal coming from the common mode detector further discussed.

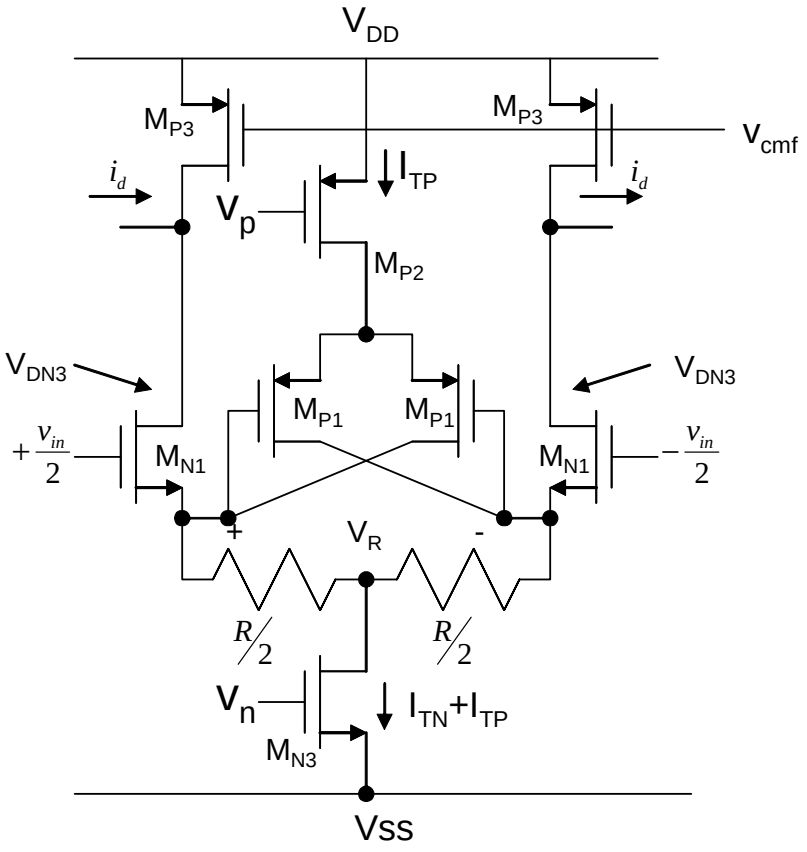


Fig. 3.12 OTA design.

The output noise of the circuit is the noise of the differential pair plus the noise of transistors M_{P3} (the noise contribution of transistors M_{p1} is negligible), then the noise factor is approximately given by:

$$\varepsilon \approx 1 + \frac{g_{mP3}(1+N_r)}{g_{MN1}} \quad (3.29)$$

where $g_{mP3} \cong I_T/V_{dsatP3}$ and $g_{mN1} \cong I_T/V_{dsatN1}$ is the transconductance of transistors M_{P3} and M_{N1}. Thus (3.29) can be expressed as:

$$\varepsilon = 1 + (1+N_R)\frac{V_{dsatN1}}{V_{dsatP3}} \quad (3.30)$$

Since for our design $\varepsilon<2$, it follows:

$$(1+N_R)V_{dsatN1} < V_{dsatP3} \quad (3.31)$$

Then it is desired to V_{dsatP3} as much as possible. However, another design constraint is the voltage overhead necessary to keep the transistors in saturation region. For transistor M_{P3}, V_{DD} has to be larger than its saturation voltage to allow signal variations at its drain:

$$V_{dd} > V_{dsatP3} + V_{do} \quad (3.32)$$

where V_{do} are the output signal variations (The common mode voltage is referred to ground). To keep M_{N1} and M_{N3} in saturation, V_{SS} has to meet:

$$-V_{ss} > V_{dsatN1} + V_T + V_R + V_{DN3} \quad (3.33)$$

where V_T is the threshold voltage and V_R the voltage drop at the resistor given by:

$$V_R = \frac{RI_T}{4} \approx \frac{N_R}{4} V_{dsatN1} \quad (3.34)$$

V_{DN3} is the drain to source voltage of transistor M_{N3} and has to satisfy:

$$V_{DN3} > V_{dsatN3} \quad (3.35)$$

In order to increase the rejection to low frequency common mode signals, it is desired to maximize the drain to source resistance of transistor M_{N3} and therefore increase Vdn3 over VdsatN3 as much as possible. For this reason the supply voltages are chosen Vss=-2V and Vdd=1.3V.

The power consumption has a relation with the total transconductance of the circuit and it is given by:

$$G_M = \frac{g_{mN1}}{2(1+N_R)} \qquad (3.36)$$

Since the aim of this transconductor is to design G_M=1mA/V , $g_{mN1} \cong I_T/V_{dsatN1}$ and if we select V_{dsatP3}=1V, then from (3.30) I_T=2mA and Nr=2 for V_{dsatN1}=300mV and R=500. The current I_{TP} is set to I_T/16 and the sizes of M_{P1} are designed according to (3.22) to meet the linearity cancellation specification. Table 3.2 presents the sizes and drain to source currents of transistors for R=500Ω. For improved matching, all transistors use L=1um instead of the minimum feature size; an exception is made for M_{P3} where L=3um to improve the drain to source impedance.

The transconductor's core was simulated in Cadence and table 3.3 presents the simulation results with and without the ADP. The input referred noise with the ADP activated is 6nV and since the noise density of an equivalent conductance of 1mA/V is 4nV, the noise factor is ε=2.25 (slightly larger than calculated). The IM3 without the ADP can be computed as:

$$IM3 = \frac{3V_A^{\,2}}{128V_{dsatN1}(1+N_r)^3} \qquad (3.37)$$

Table 3.2. Transistor sizes.

Transistor	**W/L**	**Drain to source current**
M_{N1}	200µm / 1µm	1.17mA
M_{N2}	25µm / 1µm	147µA
M_{N3}	340µm / 1µm	2.5mA
M_{N4}	40µm / 1µm	295µA
M_{P1}	27.2 µm / 1µm	74µA
M_{P2}	60µm / 1µm	148µA
M_{P3}	192µm / 3µm	1.17mA
M_{P4}	48µm / 1µm	295µA

Table 3.3. OTA: simulated parameters with R=500Ω.

Parameter	**Without ADP**	**Transconductor with ADP**
Power consumption.	8 mW	8.3 mW
IM3 at 0.7Vpp 30 MHz.	-63 dB	-80 dB
Transconductance.	1.15 mA/V	1.05 mA/V
Input referred noise density.	5.4 nV/√Hz	6 nV/√Hz
IIP3.	26.4 dBm	35 dBm
Differential gain.	32 dB	32 dB
Common mode gain.	-25 dB	-25 dB
Area	0.033 mm^2	0.035 mm^2
CMRR @ 30 MHz	< -50 dB	< -50 dB
PSRR @ 30 MHz	< -50 dB	< -50 dB

With the parameters obtained for this design, an IM3 of -60dB for a 0.7Vpp is obtained which is close to the simulation result. Notice that with the addition of the ADP, the IM3 improves by 17dB with less than 1dB in noise increment. The extra area used by the ADP is less than 6%; fig. 3.13 shows the micrograph of the OTA where the small increase in area can be appreciated. The power efficiency of the circuit defined as the peak AC power over the DC power is 0.03 for an IIP3 of 35dBm.

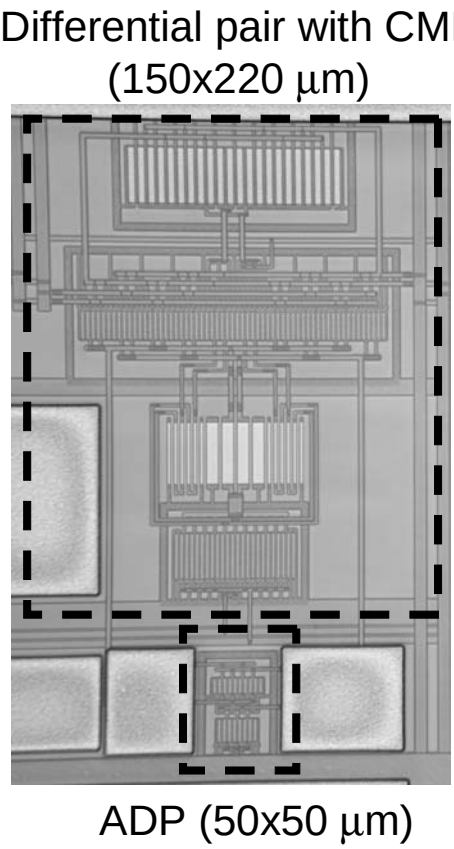


Fig. 3.13. Micrograph of the OTA.

3.2.4 Common mode feedback

Due to the differential nature of the OTA, common mode feedback is required to fix the common mode point at the output. One possible option is to take advantage of node at the drain of MN3 which inherently contains the common voltage related to the input. However, the capacitance from drain to VSS of transistor M_{N3} together with the degeneration resistance generate a pole; furthermore, since the voltage the drain of MN3 is close to VSS, a level shifter may be required to increase the voltage for better signal handling which adds up to the circuitry and creates another pole. Therefore, a simpler design is chosen with a set of two differential pairs and current mirrors incorporated to each OTA as shown in fig. 3.14.

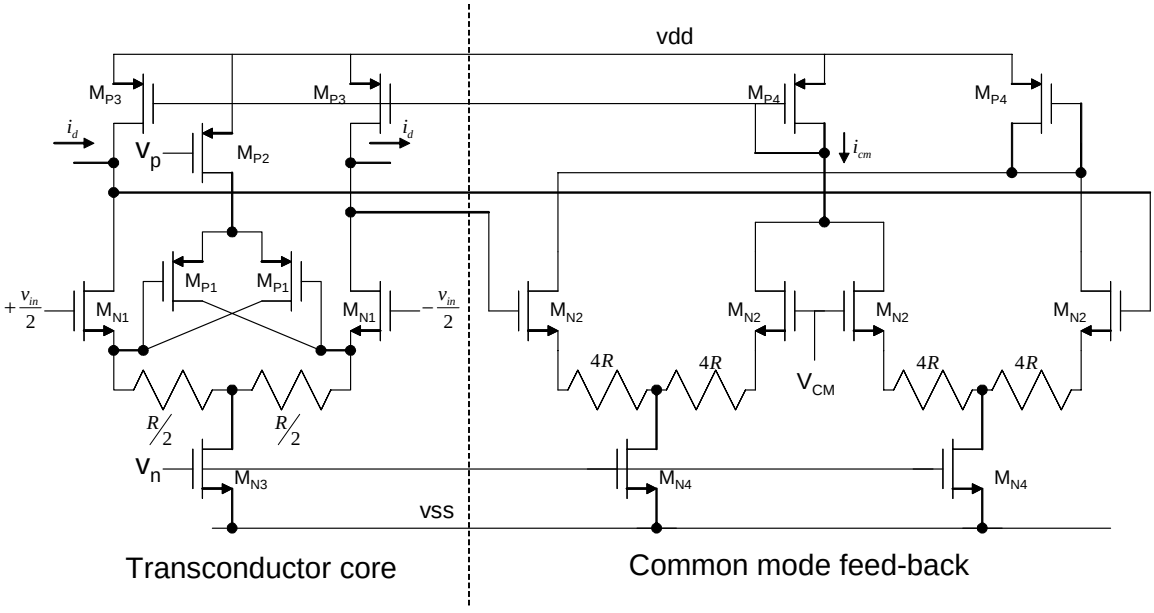


Fig. 3.14. Diagram of the OTA with the common mode feed-back.

To ensure that each differential pair can handle the input signal and to simplify the layout, transistors M_{N2} and M_{N4} share the same Vdsat as M_{N1} and M_{N3} respectively. Thus the differential pairs are a scaled version of the OTA by a factor k and the output current from the differential pairs is scaled by the ratio between M_{P4} and M_{P3}, therefore the common mode transconductance G_{CM} is given by:

$$G_{CM} = G_M k \frac{(W/L)_{P3}}{(W/L)_{P4}} \qquad (3.38)$$

As it is desired to reduce k to save the power consumption, the ratio between M_{P3} and M_{P4} can be increased to maintain a large G_{CM}. The trade-off, however, is that a parasitic pole at the gates of MP4 is reduced. The frequency of the pole is given by:

$$w_p = \frac{g_{mp4}}{C_{p4}\left(1+2\frac{(W/L)_{P3}}{(W/L)_{P4}}\right)} \qquad (3.39)$$

where C_{p4} is the gate to source parasitic capacitance of MP4. Considering the above trade off, k=¼ and a size ratio between M_{P3} and M_{p4} is selected. The resulting common mode transconductance is 1mA/V with a bandwidth of 30MHz. In open loop, the common mode feed-back circuit has a gain of 30dB and over 60 degrees of phase margin. The nominal power consumption is 2mW, one quarter of the OTA's total power.

3.2.5 Self-bias circuit

As mentioned in the previous section, it is important to maintain a fixed Nr in order to reduce the sensitivity to process variations and maintain the non-linearity cancellation condition given in (3.16). To this end, a self bias circuit is incorporated to

modulate the tail current I_{TN} of OTAs until the transconductance reaches the desired $Nr=G_{MN1}R$. The conceptual diagram of the calibration circuit is depicted in fig. 3.15.

A differential pair without source degeneration is used to extract G_{MN1} with a non-critical DC input voltage V_{REF}, then the differential output voltage is mainly determined by $V_R=G_{M1N}(nR)V_{ref}$; $n=N_r^{-1}$. A comparator senses the difference between V_R and $V_{REF,}$ then amplifies the error and injects it to the tail current. As a result, the high loop gain adjusts G_{M1N} by varying the tail current I_{TBN} until the condition $V_R=V_{ref}$ is met. A common mode feedback circuit (indicated as CMFB) maintains the output common mode voltage fixed at the reference level. Since the variations in I_{TBN} also change G_{MN3}, I_{TBP} is also proportionally modified to maintain the G_{MN3}/G_{MP3} relation almost constant and comply with (3.16). I_{TBN} and I_{TBP} are copied to I_{TN} and I_{TP} respectively in all the OTAs in the filter.

.

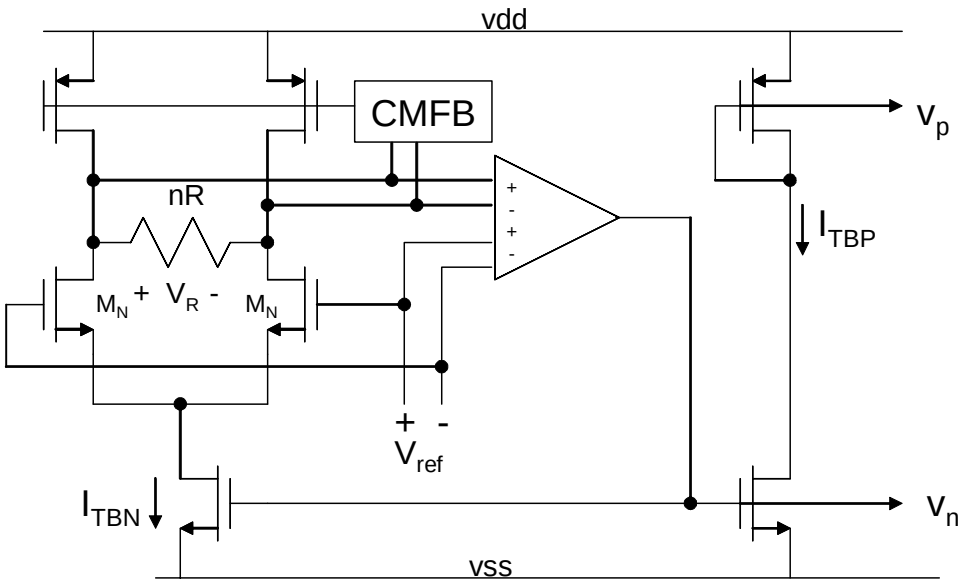


Fig. 3.15. Auto-bias circuit concept.

The differential comparator is designed as shown in fig. 3.16 with two PMOS differential pairs. The use of a PMOS structure facilitates the interface to Vn and earns one current mirror compared to an equivalent NMOS structure. When steady state is reached (V_R=V_{REF}), the input at each differential consist only in the common mode error between Vref and Vr which is very small; hence the differential pairs do not require source degeneration and high transconductance can be achieved. The comparator consumes less than 1mW and provides a loop gain of 30dB. The common mode feedback is designed with the same structure as described in fig. 3.14 except that no source degeneration is used. The total power consumption of the self-bias circuit is 3.5mW.

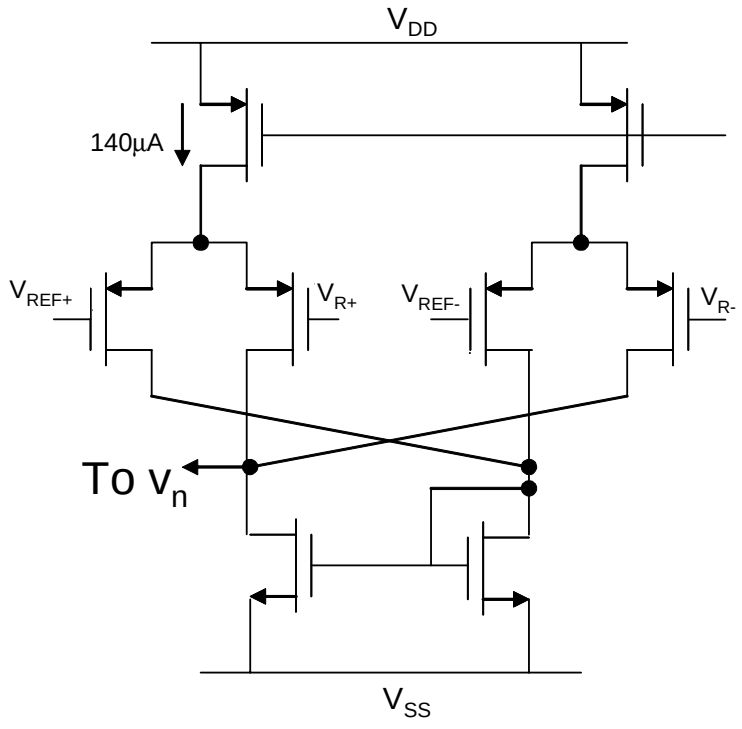


Fig. 3.16. Comparator schematic.

Offset voltages present in the comparator due to mismatch prevent the self-bias circuit to achieve the optimal bias point to achieve the best linearity. Shown in figure 3.17 is a curve showing the IM3 degradation in the presence of offset voltage. The circuit is used for proof of concept purposes, but if offset is a concern, higher reference voltage Vr can be used or chopping techniques can be incorporated.

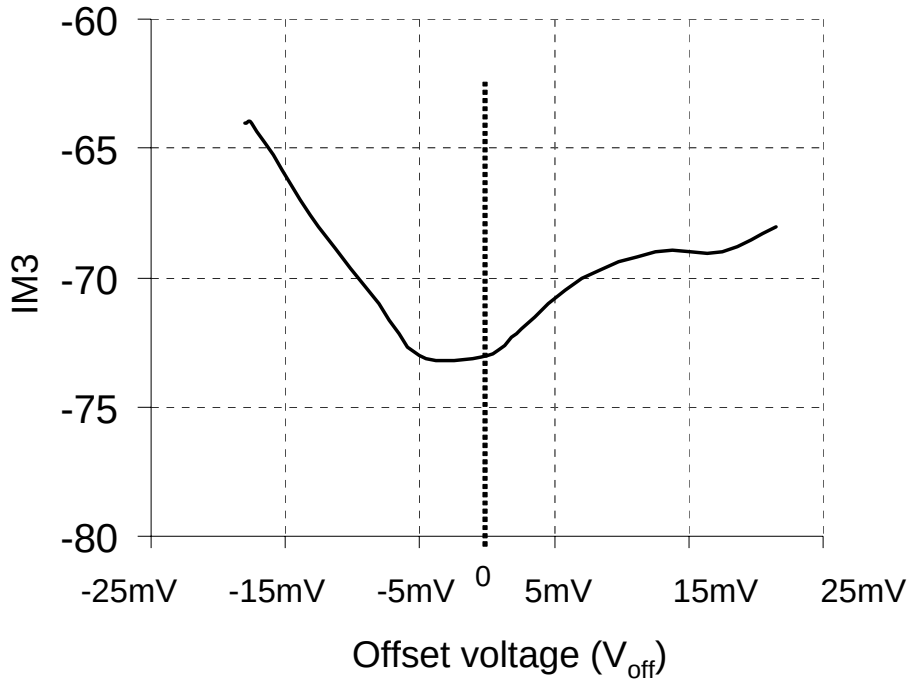


Fig. 3.17 . IM3 vs. offset voltage in the comparator (V_{off}).

3.2.6 Capacitors

In typical OTA-C ladder realizations, terminations resistances are also implemented by transconductors and the filter's characteristic do not depend on

polysilicon resistances. In this case, thanks to the availability of a self-bias circuit the polysilicon resistance value is matched to the transconductance value of OTA's. Therefore, it is possible to use polysilicon resistors for the ladder terminations which in turn results in power savings, lower distortion and reduced noise. However, the relation between capacitances and transconductance is critical for an accurate frequency response of the filter; hence a capacitance adjustment is necessary.

Each capacitor in the filter is designed as an array of small capacitors that can be switched via a digital word. Since OTAs bias currents are not modified during tuning, the linearity properties are not affected. Figure 3.18 shows the schematic diagram of a capacitor array; five weighted capacitors are available where the biggest is always connected but signals b0-b3 can switch the transistors via transistors M_{C1}-M_{C4} to either connect or disconnect the rest of the weighted capacitors. Therefore, sixteen different values of overall capacitance are possible ranging from C to 31/16*C that results in a frequency tuning of ±30% in average steps of 4%. Table 3.4 presents the nominal values of the capacitors used in the filter (fig. 3.12) based on a nominal $R=G_M^{-1}=1mA/V$.

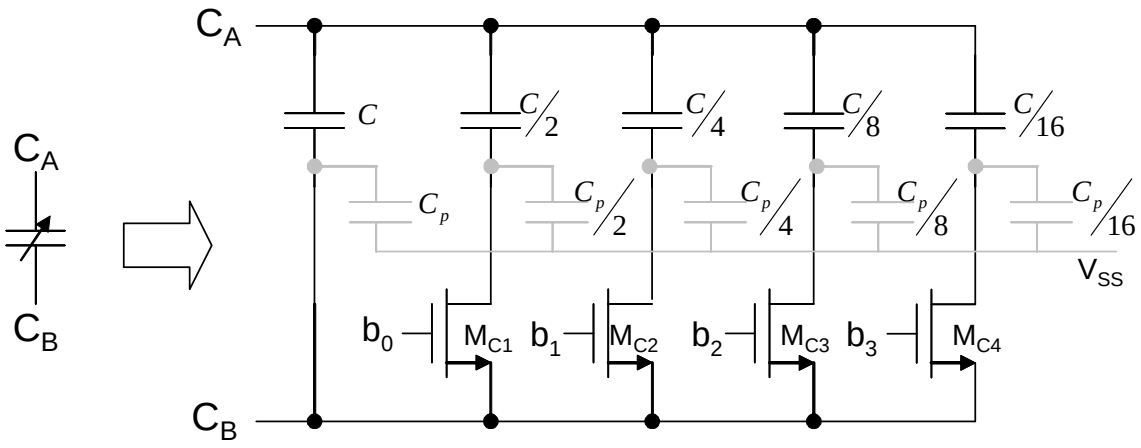


Fig. 3.18. Switched capacitor array for frequency tuning. $C_{nominal}$ = 1.5*C. On grounded capacitors C_B is connected to ground.

Table 3.4. Nominal capacitor values.

Capacitor	**Nominal value**
C_1	7.4 pF
C_2	11.2 pF
C_3	13.3 pF
C_4	6.9 pF
C_5	4.3 pF
C_6	2.3 pF
C_7	6.7 pF

Each capacitor is implemented using two parallel plates of polysilicon layers due to the good linearity and high capacitance per area. Unfortunately, as the bottom layer is close to the substrate, a parasitic capacitance C_P exists as shown with shaded lines in fig. 3.18. Typically for the technology used $C_P \approx C/8$. If the node CB is connected to ground, the effects of the parasitic capacitances are minimized; this is the case of capacitors C1-C5 in figure 3.12. However, capacitors C6 and C7 are floating and the effect of the bottom plate capacitance adds up to the capacitance at node C_B in figure 3.18; if switches are deactivated, the parasitic capacitance influence node C_A but this effect is smaller since the bigger capacitor does not use a switch. To minimize the above effect, the node CB of both floating capacitors C6 and C7 is placed towards C3 since it is the largest capacitor in the filter.

The size of transistors MC1 to MC4 on figure 3.18 used as switches, are selected such that the drain to source resistance is at least one hundred times smaller than the equivalent impedance value of the capacitor connected to the drain at 30MHz; hence their influence in the filter's transfer function is minimal.

Figure 3.19 shows the simulated post-layout AC responses of the filter for the sixteen different settings. As it can be seen, variations in the cut-off frequency from 24MHz to 40Mhz can be obtained. The non-idealities of the switching capacitors do not present a visible alteration in the roll-off shape; only the lobes at the stop-band are modified but these remain below the 30dB specified.

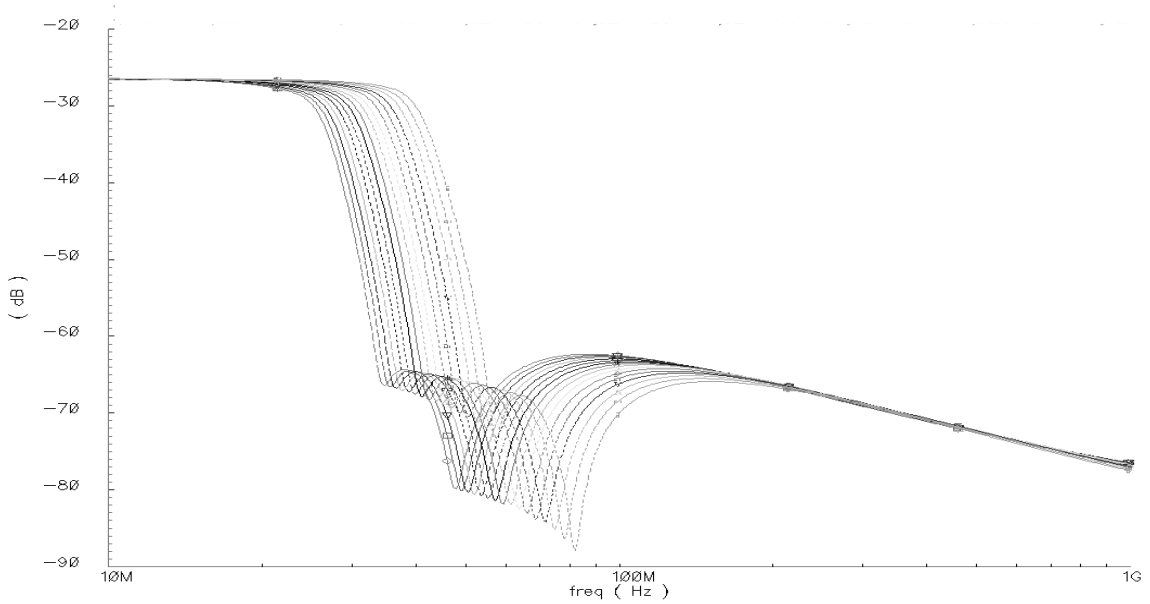


Fig. 3.19. Programmable AC responses in the filter.

3.3 Automatic tuning

All the elements inside an integrated circuit are sensitive to process variations, temperature, humidity and aging. The variations in resistance, capacitance and transconductance deviate the filter's transfer function from the desired specifications. Therefore, an extra circuit is necessary to perform a calibration routine and adjust certain parameters to fit the transfer function within the desired specifications. This circuit is commonly referred as the "automatic tuning system" [40].

The automatic tuning circuit uses a reference which typically is a signal of a fixed frequency from a reliable source (e.g. a crystal oscillator). It injects this signal to a

filter (or a partial replica of the filter) and, based on the measured error with respect to the reference, tunes the frequency response.

A master-slave approach fig. 3.20, can be realized based on the fact that inside the integrated circuits, all elements have similar process values and temperature (provided they are close enough): The filter is referred as the slave section because it is controlled depending on the behavior of the master. The master is a partial replica of the filter, enough to gather the necessary error information to correct the filter. In this way, the filter does not have to be inhibited from normal operation but any mismatch between the master and slave affects may affect system precision.

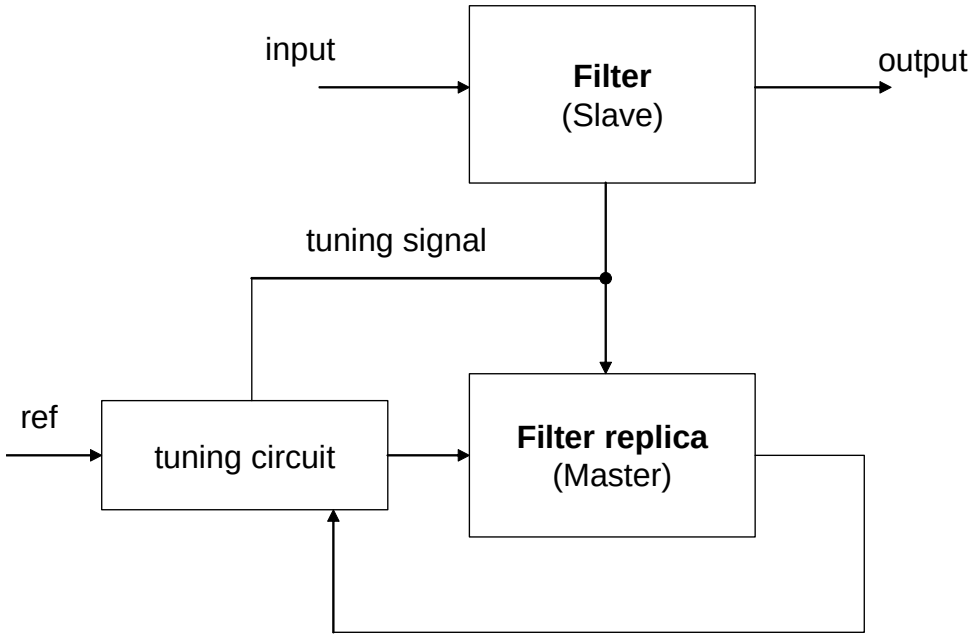


Fig. 3.20. Master-slave approach.

When power consumption and area overhead is important, a simple frequency tuning approach is desired. In such cases many master circuits rely on simply matching the transconductance to capacitance ratio. A common approach is to use an OTA as an integrator and evaluate the gain at frequency w_o=Gm/C; based on the error compared to unity gain [16], the transconductance or capacitance can be varied until the error is corrected. However, a sinusoidal tone is required and, if not available, its synthesis may require further circuit overhead. Furthermore, the above system may suffer from errors related to the magnitude detection which is usually done with envelope detectors or multipliers.

The use of sinusoidal tones can be avoided by using a Phase locked loop (PLL) [41] or a charge injection approach. Since these two approaches only detect the periodicity of the signal, they do not depend on the harmonic content of the signal and the use of the input reference signal can be a square wave which is easier to generate. In the first, two or more OTAs with a capacitor are configured to act as a voltage controlled oscillator and a PLL loop adjusts the oscillating frequency until it matches the reference frequency. In a charge injection automatic tuning [42]-[44], a capacitor is switched at the reference frequency accumulating a charge that depends on the transconductance and then releasing it together with a charge reference to an integrator. The drawback is that a PLL loop requires a low-pass filter and the charge injection needs an integrator, both with very low time constants to avoid cross-talking with the slave filter. Therefore, an external capacitor is often required.

To avoid the use of external components as well as specific shape reference signals, the proposed approach uses a simple analog ramp generator circuit with a digital tuning loop. This is especially attractive in the filter described here, where capacitors already use a 4-bit digital signal to be tuned. The following subsections describe the master circuit, the digital control tuning loop and non-idealities (such as jitter, offset and parasitic capacitances) of the proposed automatic tuning system.

3.3.1 Master circuit

Shown in fig. 3.21, the analog part of the automatic tuning consists in a ramp generator using one OTA and one replica of the capacitors used in the filter. Figure 3.22 shows a typical timing waveform where two clocks in quadrature, clk1 and clk2 are used. Initially, the capacitor is connected to ground and as clk1 activates switches SW1 and SW2, the ramp is started. At the rise of clk2 the voltage of the ramp vo is compared to Vcmp and the result is latched in a flip-flop sending a digital flag; a digital one indicates that the slope is too steep whereas a digital zero the opposite. Based on the flag, a digital control circuit modifies the values a0-a3 to tune the capacitance as illustrated in block diagram given in figure 3.23. At the completion of each ramp, the outcome of the flag determines if the counter has to be increased or decreased. If the flag contains the same value as in the previous iteration, it means that the ramp is still not reaching the final value and the value of the counter is then passed to all the capacitors in the filter as well. If the flag is different from its previous state, it indicates a change of

direction in the error; therefore a final state has been reached and the counter value is not passed to the rest of the filter capacitors. The following subsection detail the design

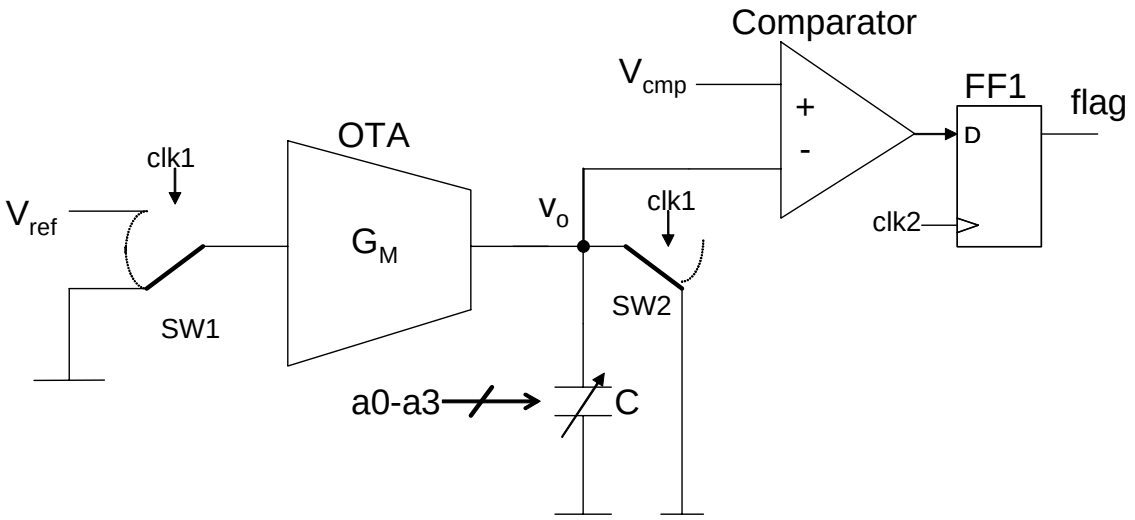


Fig. 3.21. Automatic tuning (analog section).

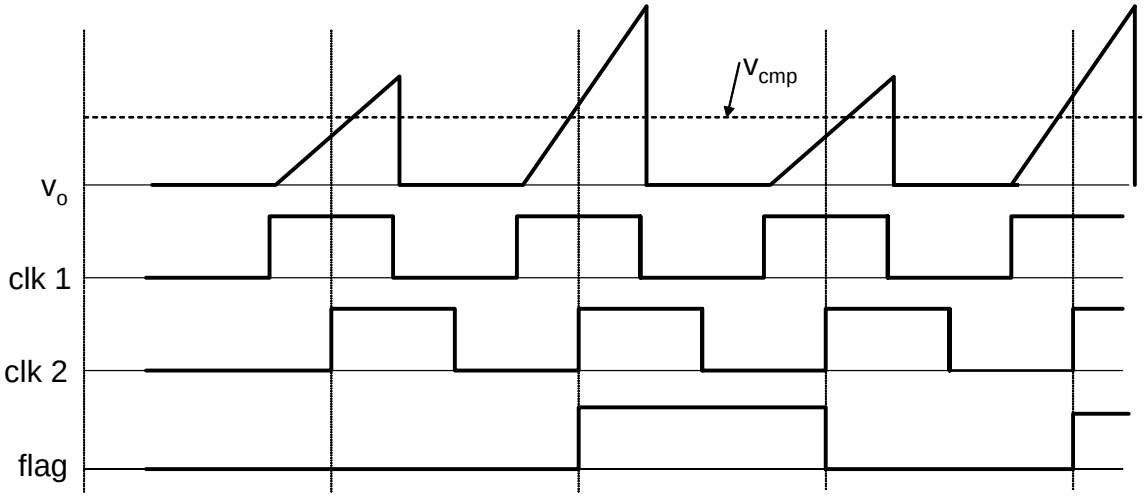


Fig. 3.22. Typical timing waveforms.

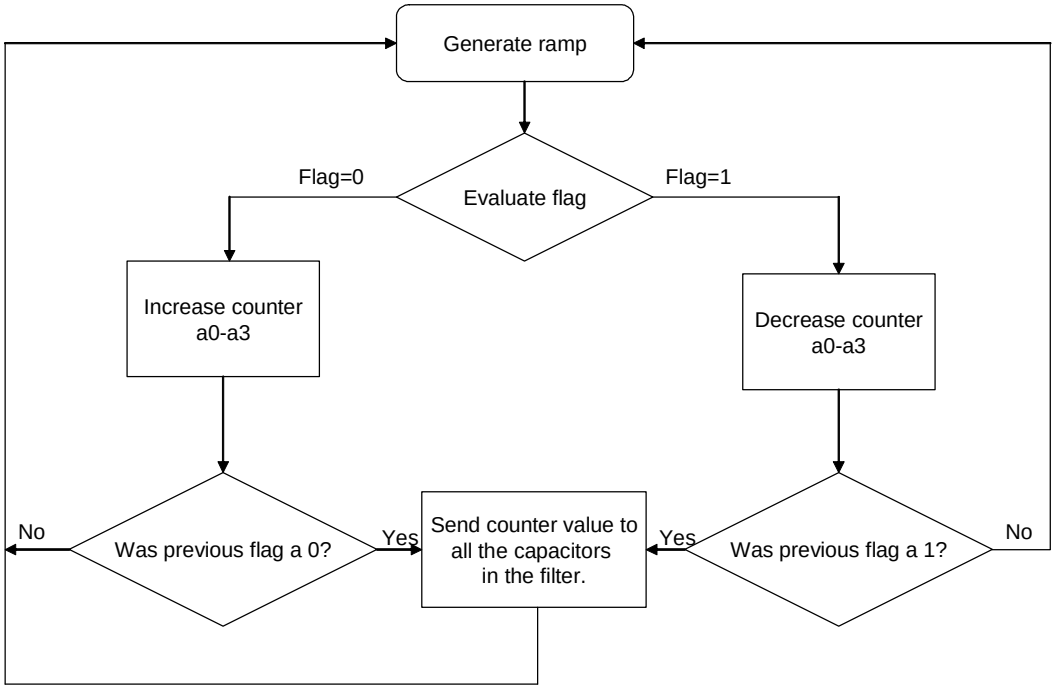


Fig. 3.23. Block diagram of the digital control loop.

3.3.1 Analog section

Since the accuracy of the tuning circuit relies on the matching between one transconductor with one capacitor (the master circuit) to the entire filter (the slave), it is important to select the most representative (or sensitive) of the capacitors to be replicated and used in the master circuit. It is possible to observe in the filter structure of figure 3.10 that there are two LC tanks formed by C6, L1 and C7, L2. For the given values for this filter topology the resonance frequencies given by $f_{res}=1/\sqrt{LC}$ are f_{res}(C6,L1)=59.81MHz and f_{res}(C7,L2)=41.3MHz. The impedance changes of a resonant LC circuit are more sensitive near the resonant frequency; since f_{res} of the resonant circuit formed by C7 and L2 is closer to the cut-off frequency of the filter, it will

introduce larger variations in the transfer function. This observation is corroborated in figure 3.24 which illustrates a sensitivity simulation performed for 20% variations in grounded capacitances for the filter implementation shown fig. 3.11. Notice that variations in C4 (that emulate the inductor L2) introduce the larger cut-off variations. Notice also that f_{res}(C7,L2) correspond to the first notch in the transfer response whereas f_{res}(C6,L1)=59.81MHz correspond to the second notch; it is then expected that the variations in the frequency of the first notch will have a greater impact in the cut-off frequency. Therefore, a copy of C4 is chosen to be used in the master tuning (figure 3.21).

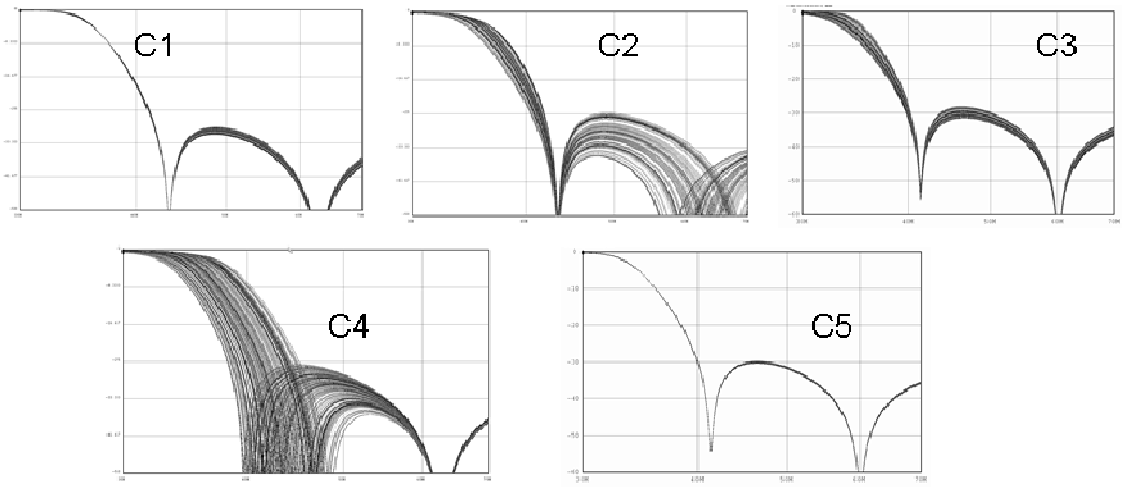


Fig. 3.24. Transfer function changes with variations in individual capacitances.

Ideally the output voltage vo in the master of figure 3.21 is given by:

$$v_o = V_{ref} \frac{G_M}{C} t \qquad (3.40)$$

where t is the duration of the ramp and the goal of the automatic tuning is to achieve a vo=Vcmp at time Tclk/2 , where Tclk is the clock period. Then from (3.40) Tclk has to be chosen such that,

$$T_{clk} = 2\frac{V_{cmp}}{V_{ref}}\frac{C}{G_M} \qquad (3.41)$$

Since the nominal value of C4 is around 7pF and Gm=1mA, the period of the clock will be 14ns for a Vcmp=Vref. As the digital rising and falling times for the used technology are close to 1nS, it may be complicated to achieve a good accuracy with such small periods. Therefore, the relation between Vref and Vcmp can be reduced for increased Tclk. However, Vcmp cannot be larger than the maximum allowed output voltage of around 1Vpp and with the use of small Vref the mismatch offset of the OTA would worsen the accuracy. Then, to increase the ramp time the OTA is modified as shown in fig 3.25 where only 1/8 of the output OTA current is directed to the capacitors; the rest is injected to ground. As a result, the OTA uses 1/8 of the nominal transconductance and since only 1/8 of the transistors are connected to the output, the resistance is eight times higher keeping the same DC voltage gain. In this way, T_{clk} can be increased eight times for Vref=Vcmp without worsening the period error. Additionally, there is no need to use a second reference voltage and Vref does not have to be precise since Vcmp=Vref.

The schematic of the comparator is shown in figure 3.26. Transistors M1 form two differential pairs to compare Vcmp to Vo. The difference in current i_{c+}-i_{c-} is the result of the comparison is mirrored into transistors M2 to reduce any kickback charge

caused by fast latch transients into the comparator. The latch is formed with cross-coupled transistors M4 and when the /latch signal becomes low, the negative resistance latches the comparison result. The total power consumption of the master circuit is 10mW.

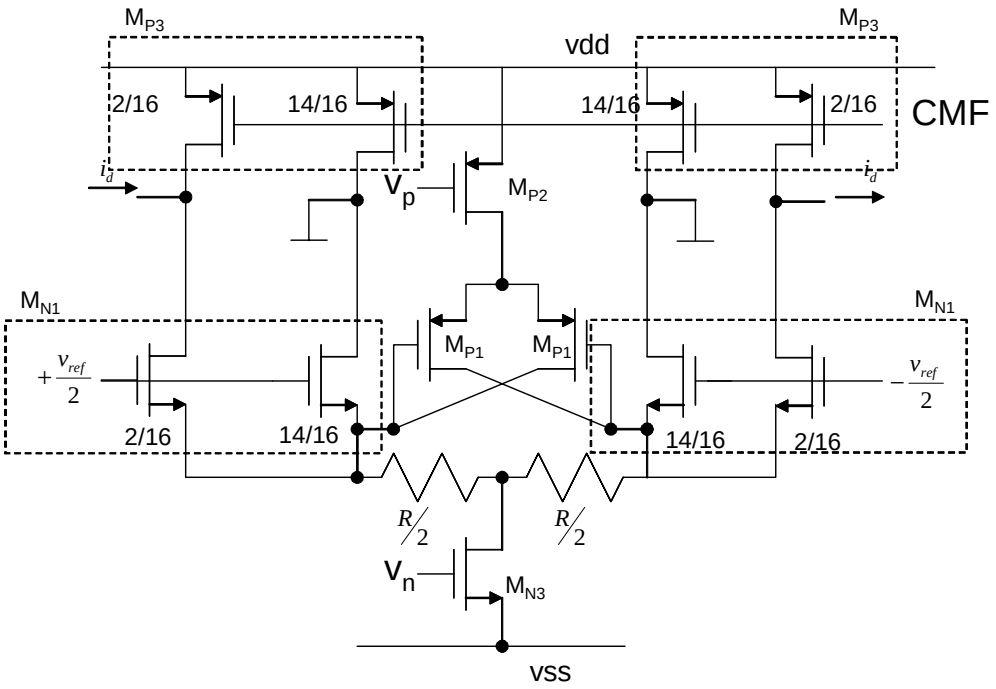


Fig. 3.25. OTA used in the automatic tuning system.

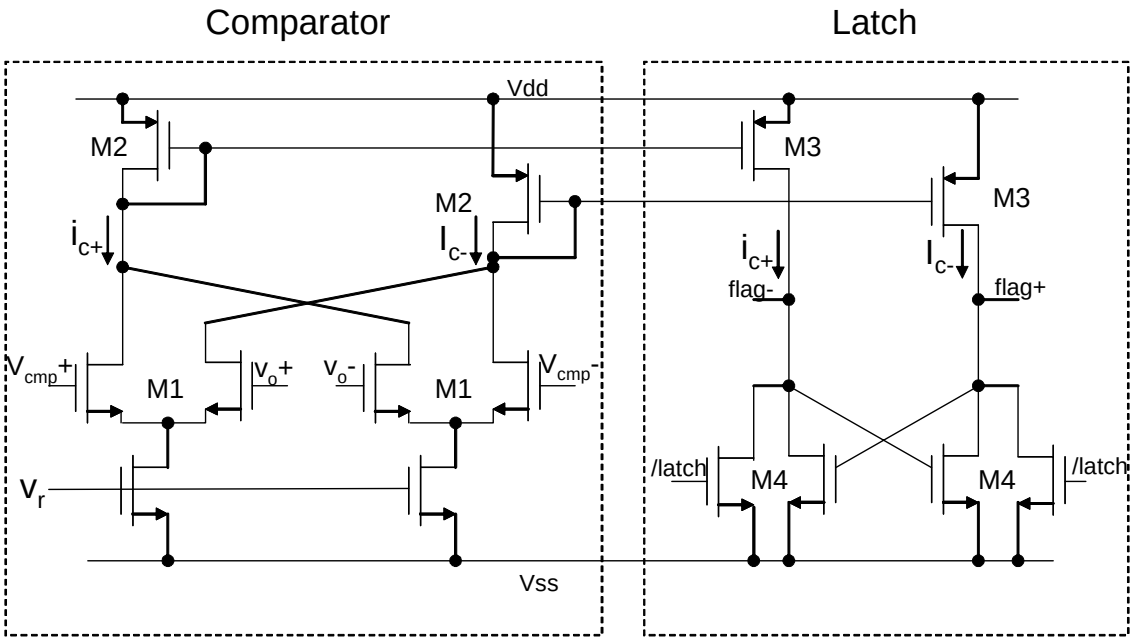


Fig. 3.26. Comparator used in the automatic tuning.

3.3.2 Digital tuning circuit

The purpose of the digital tuning circuit is to generate the necessary waveforms to drive the master circuit and after several ramp iterations, converge to a final value of capacitance based on the flag output.

Figure 3.27 shows the clock generator. From one digital external reference and using flip-flops and two inverters the circuit ensures that clk1 is 90° ahead of clk2. Figure 3.28 presents the digital control circuit. A four bit counter is used to adjust the capacitance via a0-a3 signals based on the flag indication. Once the final value has been reached, the capacitor in the master circuit cycles between two values; a combinational circuit formed with FF3, G1 and G2 detects that the final value has been reached and holds the value to the rest of the capacitors in the filter in a latch.

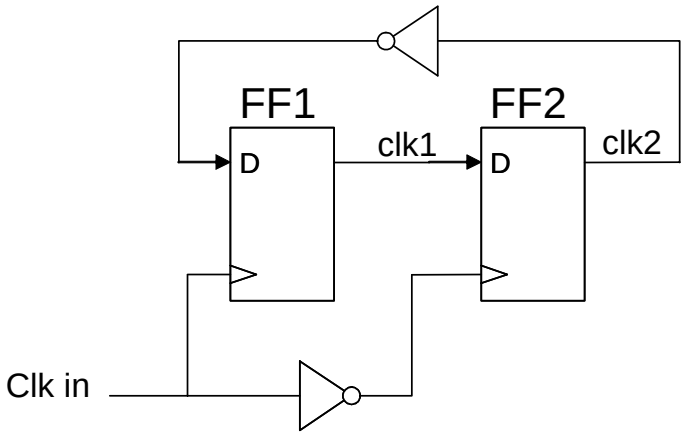


Fig. 3.27. Clock generator.

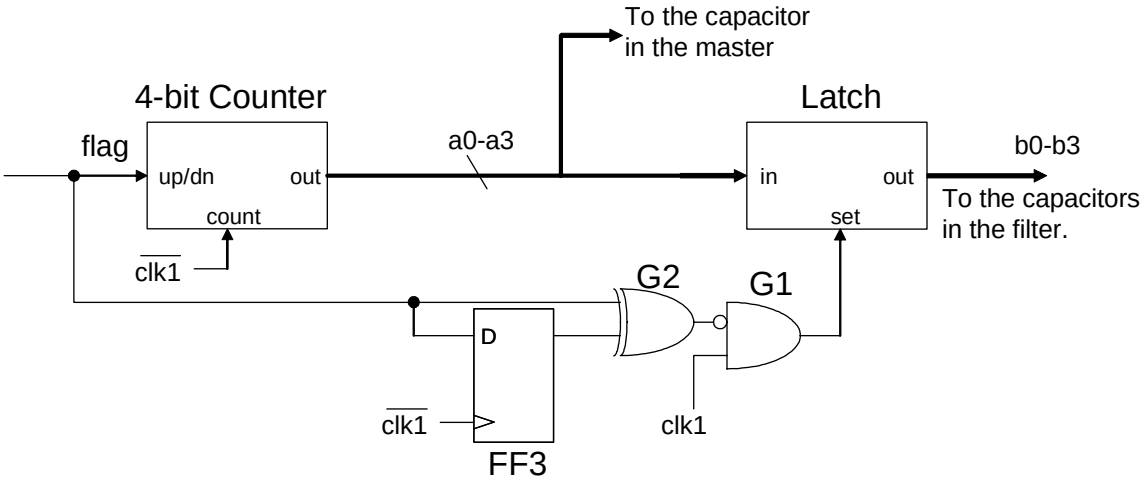


Fig. 3.28. Digital control section.

3.3.3 Non-idealities

The accuracy of the automatic tuning system can be tampered with the jitter in the clock, mismatch offset errors, the finite resistance at the output and parasitic capacitances. The effect of each of these is treated next.

3.3.3.1 Jitter and mismatch (offset)

In equation (3.41), there is a direct relation between the clock period and the capacitance value. Therefore, in a noise reference source any variations in the clock period produced by jitter can result in ramp errors. However, since jitter is a random noise, the problem can be alleviated by generating several ramps and obtain the final flag based on the averaging of previous flags.

The mismatch between the components in the OTA and the comparator, produce an input offset that add up to Vcmp and Vref. To reduce the problem, Vcmp and Vref should be made as large as possible. For a typical input offset of 10mV the error between Gm and C will be of less than ±2% according to (3.35) when Vcmp=Vref=500mV.

3.3.3.2 Output resistance

Due to the finite output of the OTA the output of the integrator is determined by an exponential curve given by:

$$v_o = V_{ref} A_{dc} \left(1 - e^{-\frac{G_M}{CA_{dc}} t} \right) \qquad (3.42)$$

where Adc is the DC gain of the OTA. If Adc tends to infinity then (3.42) yields (3.40).

However, for a finite Adc (due to the finite output resistance) the exponential behavior creates an error in the clock period as shown in figure 3.29. The clock period of the exponential curve Texp is given by:

$$T_{\exp} = -2\frac{C}{G_M} A_{dc} \ln\left(1 - \frac{V_{cmp}}{V_{ref} A_{dc}}\right) \qquad (3.43)$$

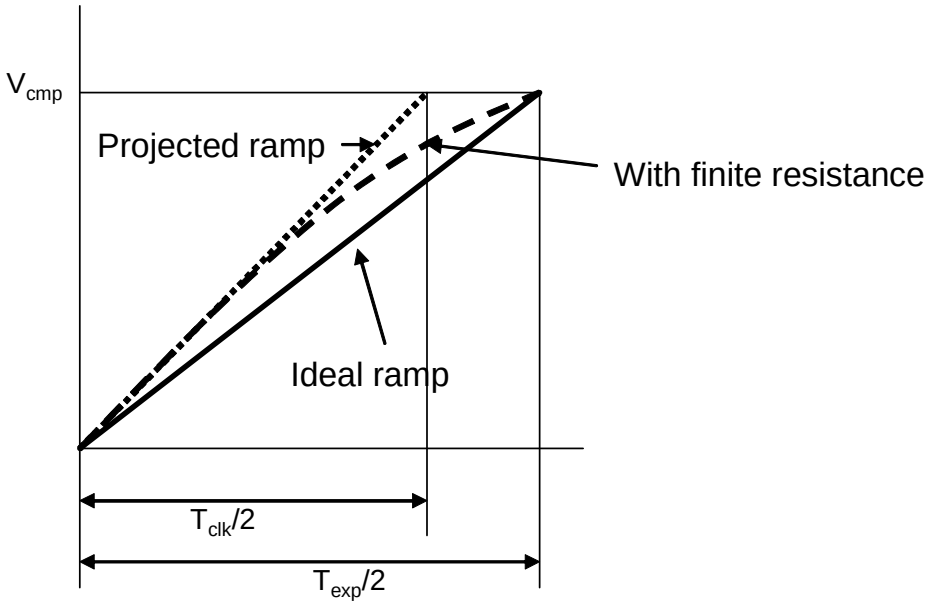


Fig. 3.29. Deviation of the ideal ramp due to the finite output resistance.

The frequency tuning error is proportional to the time error between the ideal ramp and the projected ramp due to the output resistance. This error in error is given Terr as:

$$T_{err} = \frac{T_{\exp} - T_{clk}}{T_{clk}} \qquad (3.44)$$

where T_{clk} is the projected ramp (or the slope at time 0 of the non-ideal ramp) with period as given in (3.40). Then, with (3.43) it follows:

$$T_{err} = 1 + A_{dc} \frac{V_{ref}}{V_{cmp}} \ln\left(1 - \frac{V_{cmp}}{V_{ref} A_{dc}}\right) \qquad (3.45)$$

It is difficult to gather any insight from (3.45) due to the logarithmic form. To simplify the result, the second term of (3.45) can be expanded in taylor series considering the first two terms only. Then, (3.45) becomes:

$$T_{err} \approx \frac{V_{cmp}}{2V_{ref}A_{dc}} \qquad (3.46)$$

Since the gain of the OTA is around 32dB (Table 4.2), the period error for Vcmp=Vref is only around 1% which is acceptable in our scheme. Also notice in (3.46) that another reason for which it is not desired to reduce Vref in comparison with Vcmp since it increases the period error.

3.3.3.3 Parasitic capacitances

One of the non-ideal characteristics of an OTA is that it presents parasitic capacitances that modify the desired transfer function of the filter. In the filter described in fig. 3.12 there are five rows of OTAs with equal connections between terminals and Figure 3.30 shows one of these OTA pairs with input capacitances Ci, output capacitances Co and input to output capacitances Cf. The circuit can be further simplified by noting that capacitors Cf can be referred to ground; for example, observe that there is a capacitor Cf between V_{a+} to V_{b+} and from there another one to V_{a-}, then, since $V_{a+} = -V_{a-}$ the current transferred into V_{b+} is zero (or a virtual ground). The same happens from Vb into Va.

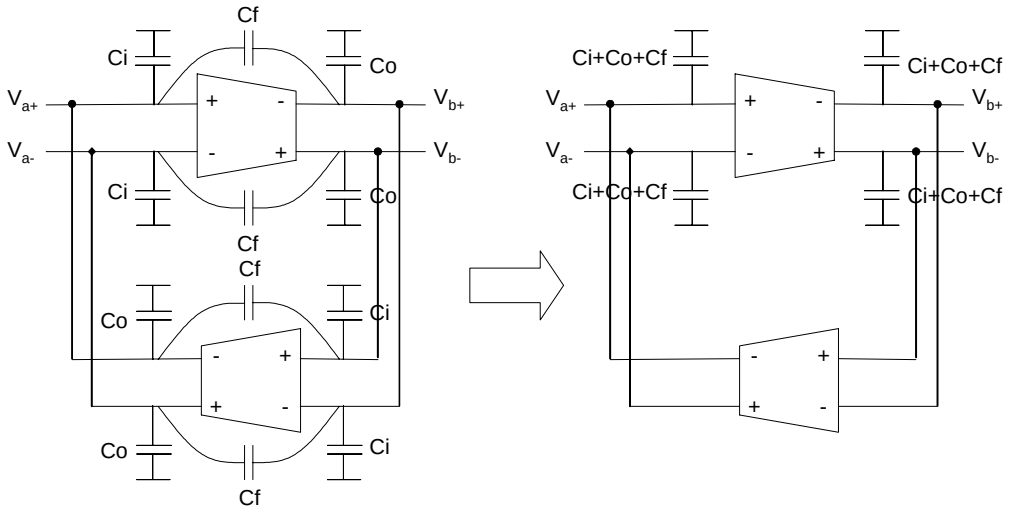


Fig. 3.30. Parasitic capacitances in an OTA pair.

Simulation results show that Ci+Co+Cf ≈ 500fF. Although this capacitors are small compared to C1 to C5 (20% of the smallest one) ,these parasitic capacitances add up and have to be taken into consideration. Therefore, an accurate Tclk that tunes the filter into the specifications is obtained via simulation rather than from equation (3.41) to account for parasitic capacitances. In this case Tclk=110ns. Unfortunately, process parameter variations can change the parasitic capacitances and further introduce an error in the automatic tuning circuit.

3.3.4 Overall accuracy

To show the effectiveness of the tuning circuit, simulation results in fig. 3.31 show changes in the cut-off frequency due to ±20% variations of polysilicon resistances with and without the automatic tuning system; the frequency error is around ±3% whereas without the automatic tuning system it is more than ±20%. However, the

precision can be further decreased when considering a 2% mismatch between transconductors, capacitors and 10mV offset errors. Figure 3.32 shows the results of the center frequency variations with the above mentioned considerations; notice that precision worsens to ±8%.

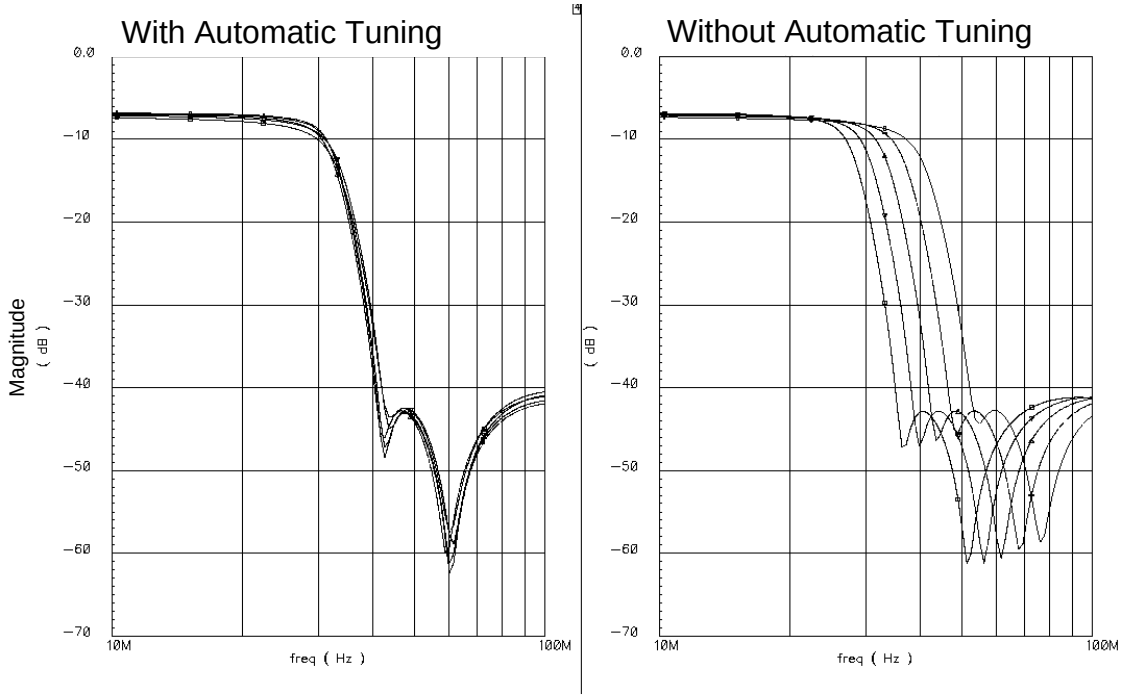


Fig. 3.31. Variations of the magnitude response with and without automatic tuning.

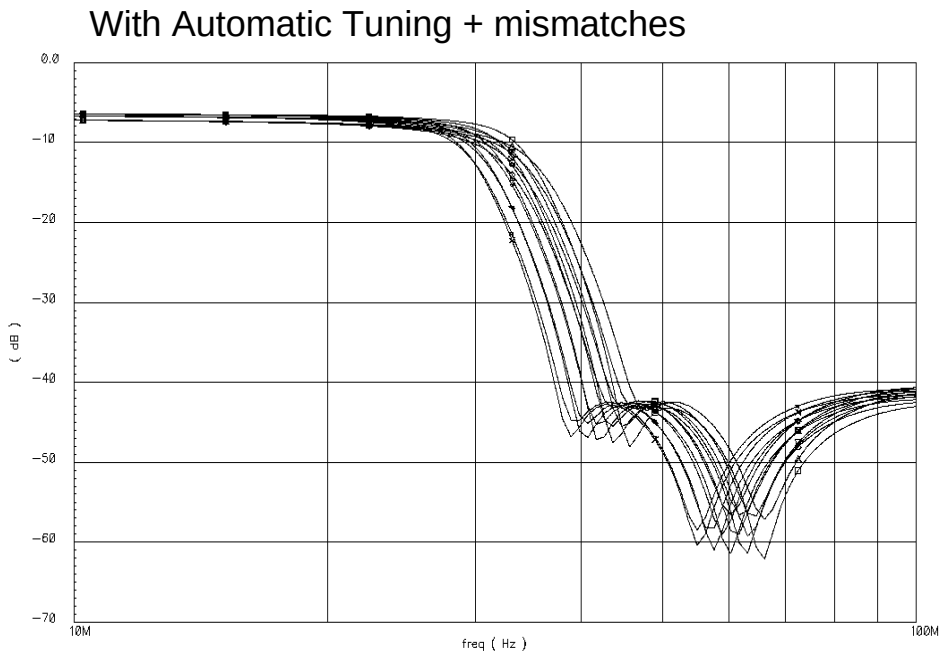


Fig. 3.32 Variations of the magnitude response with automatic tuning and mismatches.

3.4 Experimental results

The filter was fabricated in the TSMC 0.35μm process through the MOSIS service. Fig. 3.33 shows the micrograph of the chip where the total active area is 1.4mm^2 with 30% is used by the OTAs, 60% by the capacitors and 10% by the bias circuitry.

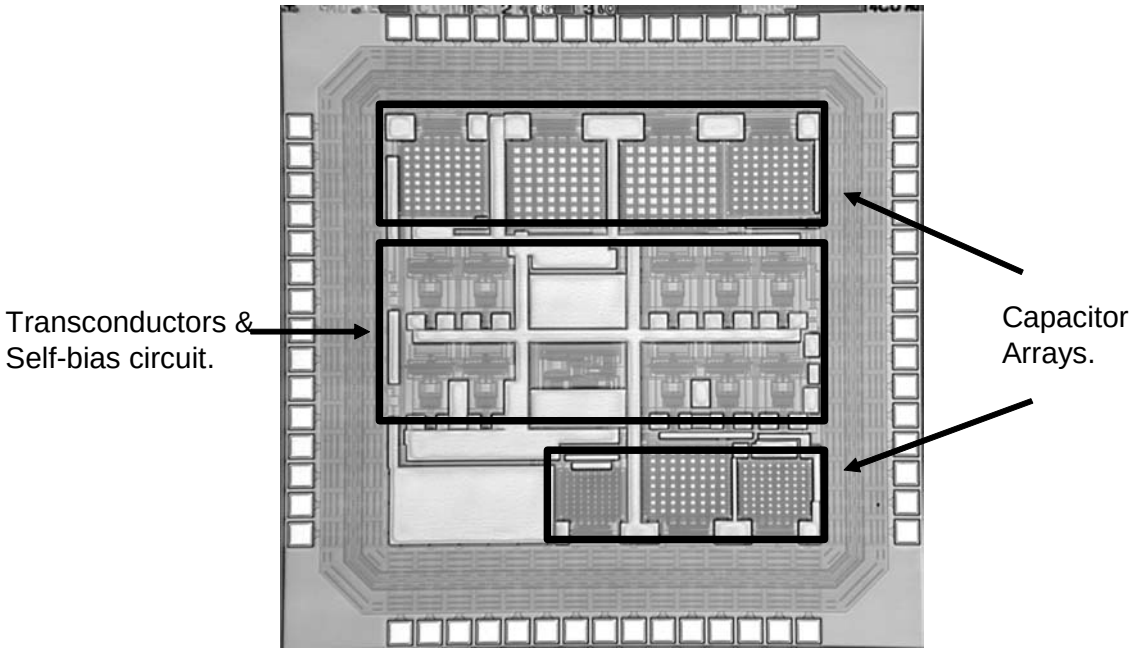


Fig. 3.33. Micrograph of the chip.

Figure 3.34 shows the test set-up. To be able to measure the output of the filter, an additional OTA inside the integrated circuit is used acting as a buffer. Simulation results show that this buffer has no impact on the filter's linearity. Baluns are used to convert signal-ended to differential signals and vice-versa. The buffer attenuates the output signal by a factor of around 26dB. Using an external signal, it is possible to deactivate the ADP in the OTA in order to evaluate the improvement with the proposed technique The AC response, linearity and other parameters were measured and described in the next subsections.

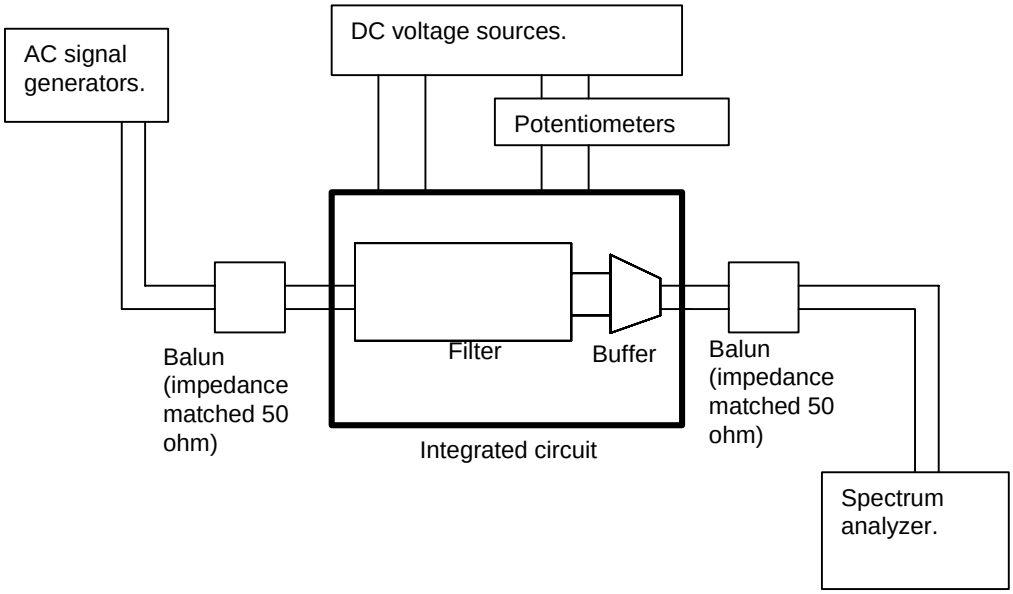


Fig. 3.34. Test set-up.

3.4.1 Frequency response

Figure 3.35 presents the low-pass responses that can be programmed in the filter. The frequency control is done by a digital word of 4 bits that result in sixteen cut-off frequency variations from 20 to 33MHz. The shape of the response coincides with simulation results with a roll-off of approximately 30dB per octave and stop band rejection of more than 30dB. Also notice that in comparison with the simulated responses shown in fig. 3.19, the control range shifted from 24-40Mhz to 20-33MHz. The reason for this deviation, is that the sheet resistance used to implement polysilicon resistors is higher than the one considered in the simulation; therefore the transconductance of OTAs is smaller than expected shifting the tuning range to lower frequencies. Still, the specified frequency of 30MHz can be tuned in this range.

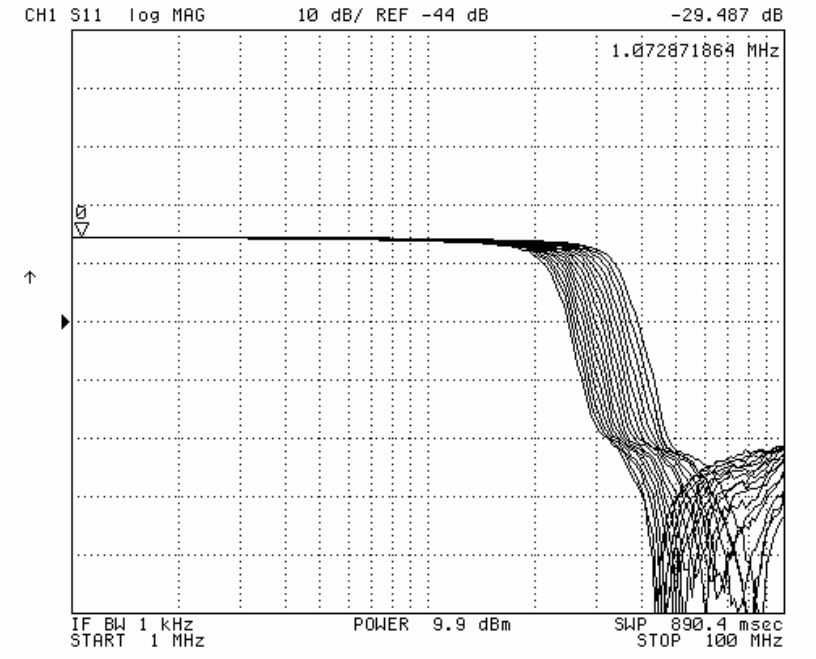


Fig. 3.35. Measured AC responses.

3.4.2 Linearity

For the linearity test, the third order intermodulation distortion (IM3) was measured at the filter output using two tones of 0.5 Vpk-pk each around 20.5MHz at the input. Figure 3.36 shows the spectrum at the output. Two shifted graphics are overlapped for comparison; the tones indicated with arrows correspond to the test with the ADP activated. In both cases the power consumption is almost the same, but for the case with ADP enabled the IM3 is 10dB lower with only 1dB of transconductance loss. Signal to distortion ratio increases by 10dB while the signal to noise ratio is almost the same.

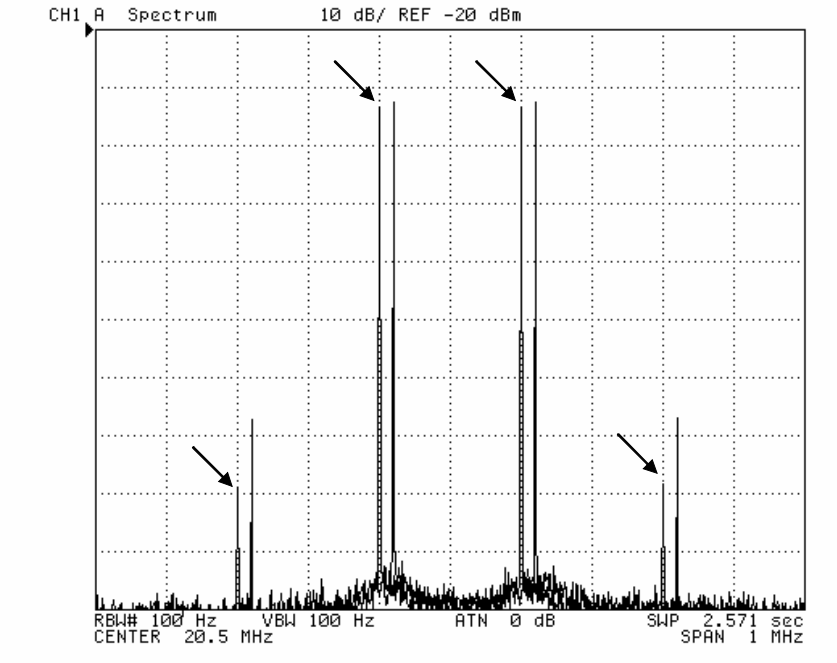


Fig. 3.36. Intermodulation tests at 20MHz.

The IM3 test was carried out for several frequencies within filter's passband; experimental and simulation results are plotted in fig. 3.37. Two sets of curves are shown for comparison (with and without ADP). If the ADP is enabled, IM3 is around 10dB lower for all frequencies. Simulation and experimental results are in good agreement.

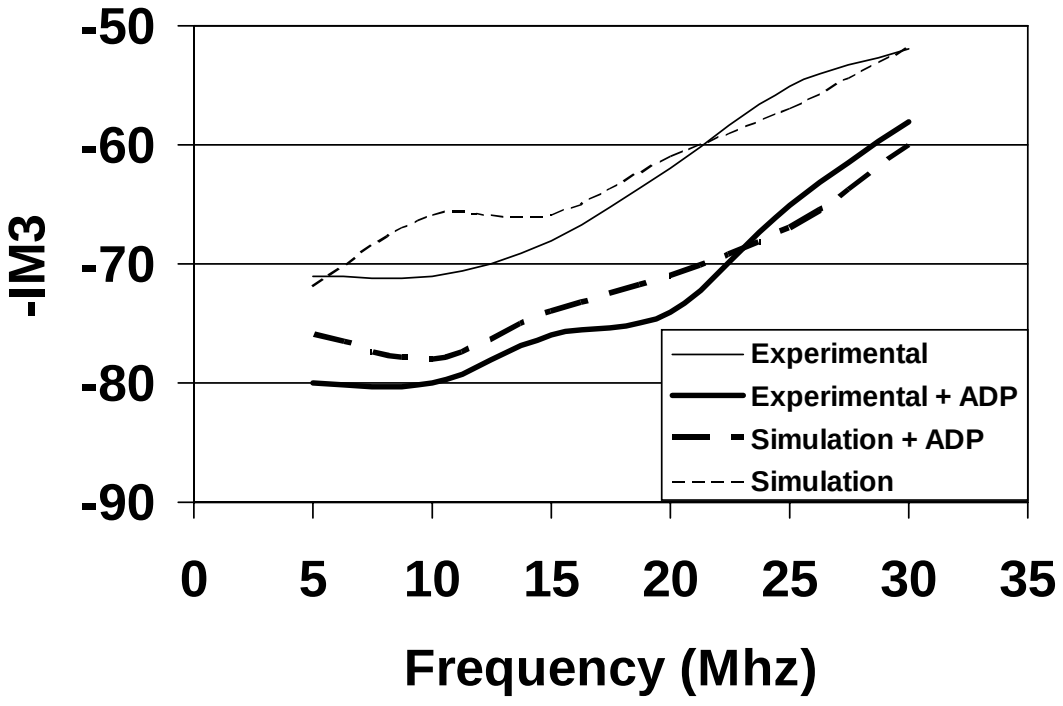


Fig. 3.37. IM3 vs. frequency.

The increase of distortion at higher frequencies is due to the following reason: The inband filter's gain is not constant but increases at high frequencies as shown in figure 3.38 (Node names relate to the filter structure presented in figure 3.11) It is then expected that the peaking at some internal nodes might degrade filter's linearity around the cut-off frequency. This effect is less important in low-Q filters such as Butterworth approximations, however, these require higher order filters compared to elliptic filters, hence more power consumption would be needed.

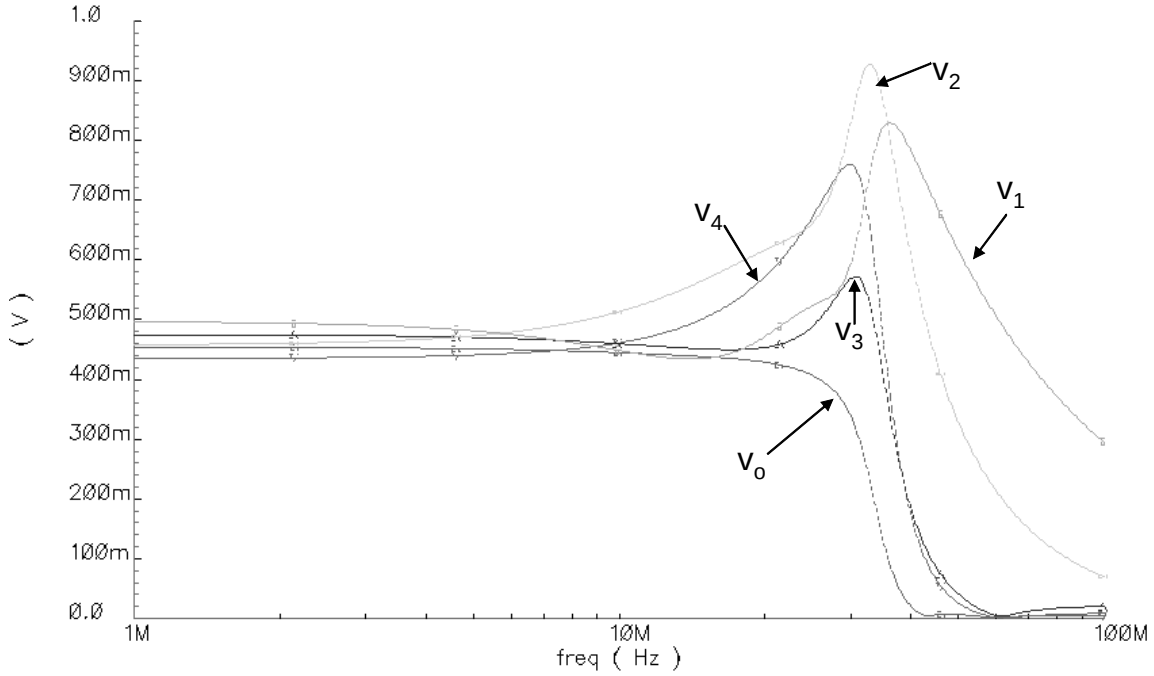


Fig. 3.38. Internal node AC response.

The out of band linearity was measured following the approach reported in [23]. Two out of band tones at 40MHz and 50MHz of 0.5 Vpk-pk each were used and the harmonic component at 30MHz was measured, leading to an IM3 of -76dB. The experimental results are shown in figure 3.39. For far out of band interferers (at 60MHz and 100MHz) the measured IM3 at 20 MHz is -90dB. Therefore, the interferers (out of band signal) create less distortion components than in-band signals.

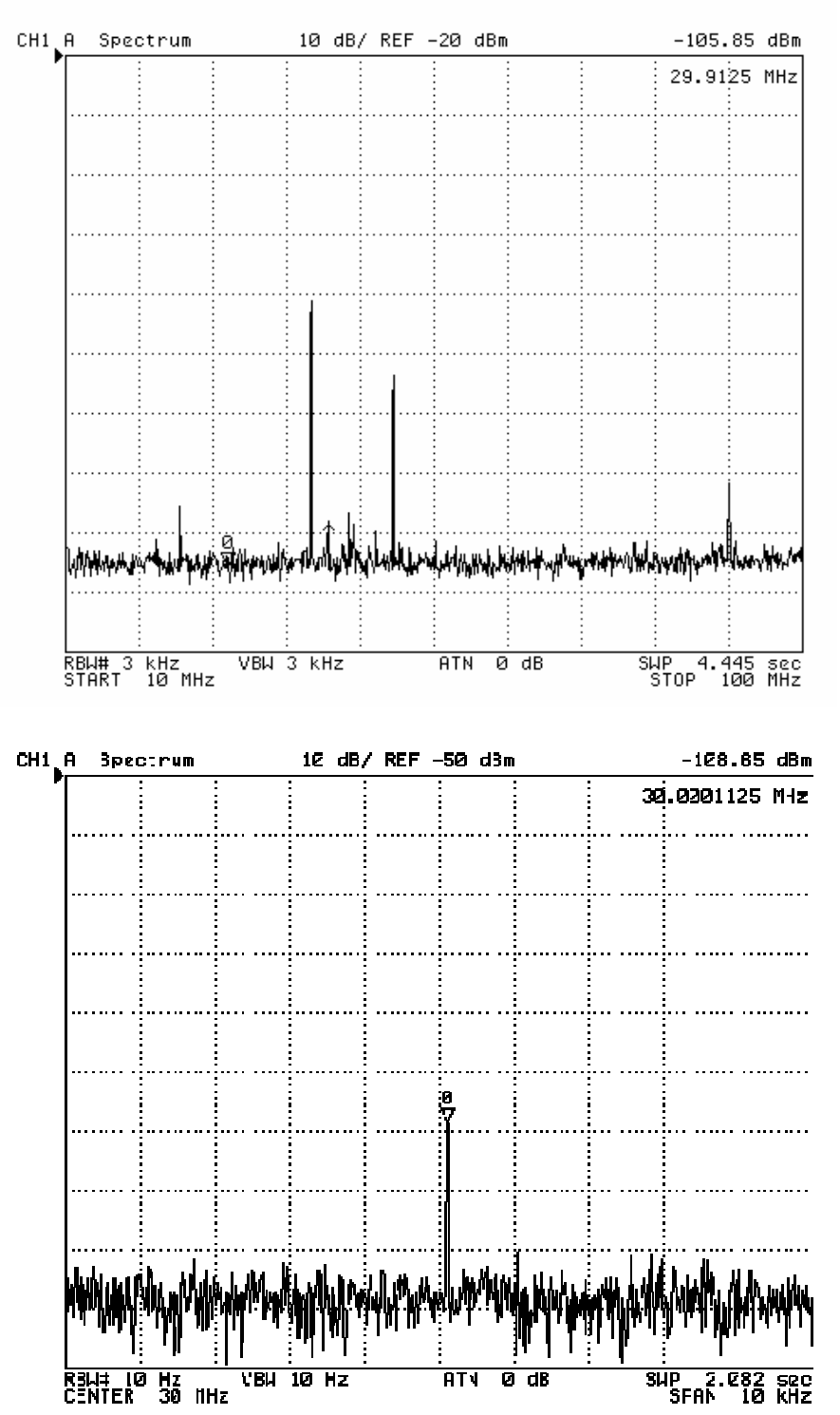


Fig. 3.39. Out of band IM3 test.

3.4.3. Noise and power

The total power consumption of the filter is 85mW. There are 9 OTAs in the circuit (8 in the filter and 1 in the self-bias circuit), then the power per OTA is around 9.5mW which is close to the estimated 10mW.

The measured total in-band input referred noise is 115μV (or 25nV/√Hz input referred noise density). Since our goal was to achieve no more than 25nV/√Hz, the filter is within specifications. For an input voltage of 1Vpk-pk, the SNR is 67dB while IM3 < -60 dB. The spurious free dynamic range is then 65dB.

Table 3.5 summarizes the experimental results and compares it with the estimated theoretical results. In general, the filter meets all the desired specifications an it is in good agreement with calculated and simulation results.

3.5. Comparison with state of the art solutions

With the proposed linearity technique, the IM3 can be improved by 10dB whereas the noise and power consumption remain almost unaltered. Since the OTA design relies on a simple differential pair without additional output stages (e.g., cascades), the noise performance is very good. Thanks to the self-bias circuit, it is possible to use polysilicon resistor for the filter terminations which presents an advantage in linearity and noise over those solutions using OTAs to emulate resistors [11]-[20].

Table 3.5. Summary of experimental results.		
Parameter	**Estimated**	**Experimental results**
Power consumption (Filter+ bias circuit)	90 mW	85 mW
Supply voltage	3.3 V	3.3 V
Input referred noise	< 135 μV	115 μV
IM3 @ $1V_{pk-pk}$, 20 MHz	< -60dB	-75 dB
IM3 @ $1V_{pk-pk}$, 30 MHz	< -60dB	-60 dB
IM3 @ $1V_{pk-pk,}$ 40MHz, 50MHz. (near out-band)	< -70dB	-76 dB
IM3 @ $1V_{pk-pk}$, 60MHz, 90MHz. (far out-band)	< -70 dB	-90 dB
SNR @ $1V_{pk-pk}$ input	> 60dB	67 dB
SFDR @ 30 MHz	> 60dB	65 dB
PSRR+	-	40 dB
PSRR-	-	30 dB
Tuning range	24-40 MHz	20-33 MHz
Linearity improvement with proposed technique.	>= 10dB	11 dB

It is very difficult and perhaps impossible to come up with an absolute figure of merit to compare one filter to another. Different filters are intended for a variety of applications that require different features; for example: a very linear phase, gain boosting, high quality factors (Q), etc. Furthermore, filters reported in the literature do not release all the results and consideration making it hard to gather enough data.

However, a good estimate can be obtained by considering the linearity, noise, power and the order of the filter which give us an idea of the dynamic range performance per power. Then, to compare this filter with previous reported solution the following figure of merit is used [9]:

$$FoM = SFDR - 10\log(P/n_p) \qquad (3.47)$$

where SFDR is the spurious free dynamic range, P the power of the filter and no the order. Figure 3.40 shows the FoM versus frequency of operation. Implementations other than Gm-C are included [21]-[24]. The trend line is plotted indicating a decaying behavior as frequency increases. This is due to two facts: larger bandwidths have larger noise and many linearity techniques can only be effective at low frequencies. Although this is a high-Q elliptic filter, its performances outperform the trend line by 6dB.

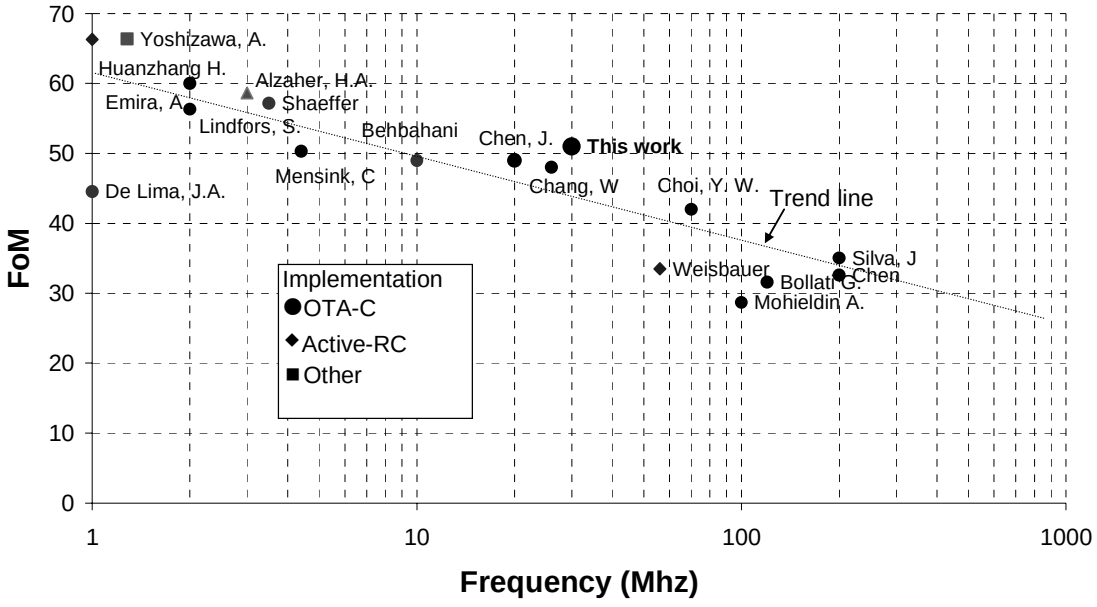


Fig. 3.40. Figure of merit of recently reported filters vs. frequency.

4. CONCLUSION

In this dissertation, three proposed OTA linearity enhancement techniques for the implementation of high dynamic range continuous time filters were presented. The first two are based on parallel cancellation using multiple differential pairs (the double and triple differential pair) and the third one is based on non-linearity source degeneration.

With the double differential pair, the IM3 can be improved more than 10dB for the same transconductance, power consumption and saturation voltage. However, it has been shown that the cancellation of non-linearities is very sensitive to process variations and difficult to compensate. An OTA based on the double differential pair was shown, where linearity independent transconductance control is featured for continuous tuning. A second order 20 MHz low-pass filter was built with identical OTA's including one extra TOTA are for external linearity tuning. With the access to the input and output of the TOTA, the bias conditions are adjusted for optimal linearity and this in turn optimizes the linearity of the entire filter regardless of the process parameter variations. The filter achieves -65dB of IM3 for 1Vpp inputs.

The triple differential pair technique, exploits the differential nature of the differential pair to divide the input by two. Then, a robust cancellation of non-linearities can be achieved regardless of process variations. The drawback is that there is a transconductance loss of 10dB. However, BSIM simulation results show that the proposed circuit exhibits better performance compared with common source degenerated differential pairs; high linearity can be achieved using moderate source degeneration

resistors resulting in lower noise, better common mode rejection and higher frequency response. Experimental results of the proposed circuit in CMOS 0.35μm show that IM3<-70dB at 1.3Vpp input for frequencies up to 70MHz.

The non-linear degeneration technique can improve IM3 by 10dB compared with the source degenerated structure, without significant loss in transconductance and SNR and the same power consumption. A self-bias circuit is used to match polysilicon resistance values to OTA's transconductance. This serves two purposes: i) minimizes the sensitivity to process variations allowing an improvement in linearity, and ii) the use of polysilicon resistive termination instead of emulating them with transconductors; this represents benefits in power consumption, noise and linearity.

A 5^{th} order low-pass elliptic filter with 65 SFDR consuming 85mW of power is presented. The frequency is tuned using arrays of capacitors without using extra power consumption and without degrading OTA performances. An automatic tuning based on a simple ramp generation maintains the frequency response tuned within ±3%. Experimental results of the circuit fabricated in a CMOS 0.35μm are presented and compared to recently published solutions; it is shown that a figure of merit based on SFDR per power is above the trend-line by 6dB.

REFERENCES

[1]. F. Behbahani, A. Karimi-Sanjaani, W. Tan, A. Roithmeier, J. Leete, K. Hoshino, and A. Abidi, "Adaptive analog IF signal processor for a wide-band CMOS wireless receiver," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1205-1217, Aug. 2001.

[2]. F. Maloberti, "High-speed data converters for communication systems," *IEEE Circuits Syst. I*, vol. 1, pp. 26-36, Jan. 2001.

[3]. S. K. Mitra and C. F. Kurth, *Miniaturized and Integrated Filters*, New York: John Wiley and Sons, July 1989.

[4]. Y. Tsividis, "Continuous-time filters in telecommunication chips," *IEEE Commun. Mag*., vol. 163, pp. 132-137, 2001.

[5]. A.Dutta-Roy, "A second wind for wiring," *IEEE Spectrum*, vol. 36, no. 9, pp. 52-60, Sept. 1999.

[6]. J. A. C. Bingham, "Multicarrier modulation for data transmission: An idea whose time has come," *IEEE Commun. Mag.*, vol. 28, pp. 5-14, May 1990.

[7]. V. Tarokh and H. Jafarkhani, "On reducing the peak to average power ratio in multicarrier communications," *IEEE Trans. Commun.*, vol. 48, pp. 37-44, Jan. 2000.

[8]. E. Schaumann, and M.A Tan,.; "The problem of on-chip automatic tuning in continuous-time integrated filters" presented at 1989 IEEE International Symposium on Circuits and Systems, 8-11 May 1989. vol.1, Pages: 106 – 109.

[9]. D. Johns and K. Martin, *Analog Integrated Circuit Design*, New York: Wiley, 1996.

[10]. D. K. Shaeffer, A. R. Shahani, S. S. Mohan, H. Samavati, H. R. Rategh, M. del Mar Hershenson, X. Min, C. P. Yue, D. J. Eddleman and T. H. Lee, "A 115-mW, 0.5-μm CMOS GPS receiver with wide dynamic-range active filters," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2219-2231, Dec. 1998.

[11]. G. Bollati, S. Marchese, M. Demicheli and R. Castello, "An eighth-order CMOS low-pass filter with 30-120 MHz tuning range and programmable boost," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1056-1066, July 2001.

[12]. J. Silva-Martinez, J. Adut, J. Rocha-Perez, J.M. Robinson and S. Rokhsaz, "A 60-mW 200-MHz continuous-time seventh-order linear phase filter with on-chip automatic tuning system," *IEEE J. Solid-State Circuits*, vol. 38, pp. 216-225, Feb. 2003.

[13]. A. A. Emira and E. Sanchez-Sinecio, "A pseudo differential complex filter for Bluetooth with frequency tuning," *IEEE Trans. Circuits and Syst. II*, vol. 50, pp. 742-754, Oct. 2003

[14]. Y. W. Choi and H. C. Luong, "A high-Q and wide-dynamic-range 70 MHz CMOS bandpass filter for wireless receivers," *IEEE Trans. Circuits Syst. II*, vol. 48, pp. 433-440, May 2001.

[15]. J. A. De Lima and C. Dualibe, "A linearly tunable low-voltage CMOS transconductor with improved common-mode stability and its application to gm-C filters," *IEEE Trans. Circuits Syst. II*, vol. 48, pp. 649-660, July 2001.

[16]. S. Lindfors, K. Halonen and M. Ismail, "A 2.7-V elliptical MOSFET-only gmC-OTA filter," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 89-95, Feb. 2000.

[17]. C. H. J. Mensink, B. Nauta, and H. Wallinga, "A CMOS soft-switched transconductor and its application in gain control and filters," *IEEE J. Solid-State Circuits*, vol. 32, pp. 989-998, July 1997.

[18]. F. Behbahani, T. Weeguan, A. Karimi-Sanjaani, A. Roithmeier, and A. A. Abidi, "A broad-band tunable CMOS channel-select filter for a low-IF wireless receiver," *IEEE J. Solid-State Circuits*, vol. 35, pp. 476-489, Apr. 2000.

[19]. A. N. Mohieldin, E. Sánchez-Sinencio, and J. Silva-Martínez, "A fully balanced pseudo-differential OTA with common-mode feedforward and inherent common-mode feedback detector," *IEEE J. Solid-State Circuits*, vol. 38, pp. 663-668, Apr. 2003.

[20]. M. Chen, J. Silva-Martinez, S. Rokhsaz and M. Robinson, "A 2-Vpp 80-200-MHz fourth-order continuous-time linear phase filter with automatic frequency tuning," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1745-1749, Oct 2003.

[21]. A. Wiesbauer, M. Clara, M. Harteneck, T. Potscher, B. Seger, C. Sandner and C. Fleischhacker, "A fully integrated analog front-end macro for cable modem applications in 0.18-μm CMOS, *IEEE J. Solid-State Circuits*, vol. 37, pp. 866-873, July 2002.

[22]. H. A. Alzaher, H. O. Elwan and M. Ismail, "A CMOS highly linear channel-select filter for 3G multistandard integrated wireless receivers," *IEEE J. Solid-State Circuits*, vol. 37, pp. 27-37, Jan. 2002.

[23]. A. Yoshizawa and Y. P. Tsividis, "Anti-blocker design techniques for MOSFET-C filters for direct conversion receivers," *IEEE J. Solid-State Circuits*, vol. 37, pp. 357-364, March 2002.

[24]. H. Huanzhang and E. K. F. Lee, “Design of low-voltage CMOS continuous-time filter with on-chip automatic tuning,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 1168-1177, Aug. 2001.

[25]. H. Weinberger, "An ADSL-RT full-rate analog front end IC with integrated line driver," *IEEE J. Solid-State Circuits*, vol. 37 no. 7, pp. 857 –865, Jul. 2002.

[26]. Z.-Y. Chang, D. Macq, D. Haspeslagh, P.M.P. Spruyt, and L.A.G. Goffart, ,"A CMOS analog front-end circuit for an FDM-based ADSL system", *IEEE J. Solid-State Circuits*, vol. 30, no.12, pp. 1449 –1456, Dec. 1995.

[27]. S.S. Lee and C.A. Laber “A BiCMOS continuous-time filter for video signal processing applications,” *IEEE J. Solid-State Circuits*, vol. 33, no. 9, pp. 1373-1382, Sep. 1998.

[28]. P. R. Grey, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, New York: Wiley, 2001

[29]. C.H.J. Mensink and B. Nauta "CMOS tunable linear current divider," *Electron. Lett*. vol. 32, no. 10, pp. 889-890. May 1996.

[30]. E. Klumperink and B. Nauta, “Systematic comparison of HF CMOS transconductors,” *IEEE Trans. Circuits Syst. II*, vol. 50, no. 10, pp. 728–741, Oct. 2003.

[31]. K. Kuo and A. Leuciuc, “A linear MOS transconductor using source degeneration and adaptive biasing,” *IEEE Trans. Circuits Syst. II* , vol. 48, pp. 937-943, Oct 2001.

[32]. S. Koziel and S. Szczepanski, “Design of highly linear tunable CMOS OTA for continuous-time filters,” *IEEE Trans. Circuits Syst. I* ,vol. 49, pp. 110-122, Feb 2002.

[33]. F. Behbahani, T. Weeguan, A. Karimi-Sanjaani, A. Roithmeier and A. A. Abidi, "A broad-band tunable CMOS channel-select filter for a low-IF wireless receiver," *IEEE J. Solid-State Circuits*, vol. 35, pp. 476-489, Apr. 2000.

[34]. A. Lewinski and J. Silva-Martinez, "OTA linearity enhancement technique for high frequency applications with IM3 below -65dB," *IEEE Trans. Circuits Syst. II*, vol. 51, pp. 542-548 Oct. 2004.

[35]. W. Huang, and E. Sanchez-Sinencio, "Robust highly linear high frequency CMOS OTA with IM3 below -70dB at 26MHz", *IEEE Trans. Circuits Syst. I*, accepted for publication.

[36]. J. Chen, E. Sanchez-Sinencio, and J. Silva-Martinez, "Frequency-dependent harmonic distortion analysis of a linearized cross-coupled CMOS OTA and its application to OTA-C filters", *IEEE Trans. Circuits Syst. I*, accepted for publication.

[37]. J. Abad, A. Badenes, J. Blasco, J. Carreras, V. Dominguez, C. Gomez, S. Iranzo, J. C. Riveiro, D. Ruiz, L. M. Torres, J. Comabella, "Extending the power line LAN up to the neighborhood transformer", *IEEE Commun. Mag.*, vol. 41, pp. 64-70, Apr. 2003.

[38]. Tonne Software, "Else – the electrical filter design program from Tonne Software". Available: tonnesoftware.com/elsie.html

[39]. Schematica Software, "Schematica software 555 timer and active filter design". Available: www.schematica.com

[40]. R. Schaumann, and M. E. Van Valkenburg. *Design of Analog Filters*. New York: Oxford Press. 2001.

[41]. H. Khorramanabadi and P. R. Gray, “High-frequency CMOS continuous-time filters,” *IEEE J. Solid-State Circuits*, vol. SC-19, no. 12, pp. 939–948, Dec. 1984.

[42]. T. R. Viswanathan, S. Murtuza, V. Syed, J. Berry and M. Staszel, “Switched-capacitor frequency control loop,” *IEEE J. Solid-State Circuits*, vol. 17, no.8, pp. 775–778, Aug. 1982.

[43]. Z. Y. Chang, D. Haspeslagh, and J. Verfaillie, “A highly linear CMOS Gm-C bandpass filter with on-chip frequency tuning,” *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 388–397, Mar. 1997.

[44]. J. Silva-Martinez, M. S. J. Steyaert, and W. Sansen, “A 10.7-MHz 68-dB SNR CMOS continuous-time filter with on-chip automatic tuning,” *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1843–1853, Dec. 1992.

VITA

Artur Juliusz Lewinski Komincz obtained his bachelor's degree with honors in Electronics Engineering in 2000 at the Instituto Tecnologico de Queretaro in Queretaro, Mexico. During his bachelor's degree program he was awarded first place in the national creativity contest of the Institutos Tecnologicos and the second place in the IEEE minirobotics national contest. From 2000 to 2006 he worked towards his Ph.D. degree at the Analog & Mixed Signal Center in the Electrical Engineering department of Texas A&M University. His Ph.D. research work focused on the dynamic range enhancement of high frequency continuous time filters. During the fall of 2001 he interned at the Data Acquisition group at Cirrus Logic. His interest areas are in analog signal processing, programmable continuous-time filters and mixed-signal interface circuits.

Artur can be reached at the Department of Computer and Electrical Engineering, Texas A&M University, College Station, TX 75204. e-mail: arturl@ee.tamu.edu.